3D IC Gap Analysis: Remaining Issues, Solutions, Market Status

While the drivers for 3D ICs remain constant, the time line for its adoption continues its shift. Several technical challenges and infrastructure issues such as business logistics are delaying the full commercialization of TSV technology for 3D ICs. While great progress has been made in via formation and filling, process steps such as debonding during wafer thinning remain problematic. Improvements in process yield that lower cost are necessary. Progress has been made in design tools and methodology, but additional work is required. Low-power design of 3D IC stacks remains in the early stages. Cost-effective thermal solutions are still required. Progress in the testing area has been reported, but work is still needed. Clarity on the issue of responsibility for the assembly and logistics requires resolution. Cost/performance targets must be met, relative to available alternatives. This report examines challenges in adopting the technology today and a realistic timeframe for the high-volume manufacturing with details of each application and its requirements.

1 Introduction
2 Design Challengs and EDA Tools
    Path-finding Tools (Atrenta, E-System Design, etc.)
    EDA Tools (Ansys, Cadence, Mentor Graphics, Synopsys, etc.)
3 Assembly Challenges (micro bumps, bonding equipment, assembly process, underfill)
4 Wafer Thinning (temporary/debond materials and equipment, carrierless solutions)
5 Thermal Issues (reduced power designs, design tools, cooling devlopments)
6 Contract Assembly Service Providers
7 Test
8 Reliability
9 Infrastructure and Logistics (OSATs, foundry, roles of each)
10 Alternatives to 3D IC (2.5D interposers-silicon, glass, laminate)
11 Standards
12 Research Institutes (ASET, CEA-LETI, Ga Tech, GINTI, HDP User Group, KAIST, Fraunhofer ISM ASSID, IME, IMEC, ITRI, NCAP, RTI, SEMATECH, STARC, Si2)
13 3D IC Market Projections in units and wafers (mobile devices, high-performance GPU, FPGAs, servers, and network systems)
14 2.5D Market Projections in units and wafers (mobile devices, high-performance GPU, FPGAs, servers, and network systems)

This study provides a forecast for number of wafers and units by application with a timeline for adoption. Alternatives to 3D ICs, including the use of silicon interposers with TSVs and continued use of Package-on-Package (PoP), are described. Impediments to the adoption of the technology are presented and progress in resolving issues is discussed. Details of research programs and remaining gaps are analyzed. Includes full text report with references and a set of complimentary PowerPoint slides.

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