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2016 Outlook

If I had not attended the 2015 3D ASIP conference, my outlook for 2016 would have been less upbeat for complex packaging (2.5/3D). But this conference showed companies and their development organizations are NOT solely looking towards FinFETS and sub 20nm silicon process nodes to meet their integration, power, speed, weight, etc metrics. We are in the perfect storm: out of control costs and consumer appetite for new functionality. Neither which are supported by continued linear CMOS process scaling!

Costs

We have all seen the classical integrated device manufacturer (IDM) disaggregate into an environment driven by fabless design companies supported by an eco-system of silicon foundries, OSATs, EDA and IP companies and numerous service companies. But if you examine the established ecosystem, all are supporting the same CMOS SoC/ASIC-like solution with process node shrinks that no longer are on an 18-24 month schedule or on the same cost curve. The CMOS silicon trains were not only slowing but the costs are increasing exponentially with each new node.

New functionality

In addition, consumers are demanding additional functionality that cannot be met by homogeneous integration. Products that requires MEMS functionality for compass, altitude, movement and medical monitoring. Products requiring higher bandwidth and denser memories supporting large data transfers (i.e. HBM, HMC, 3D SSDs). Improved wireless communication A/MS and RF modules that cannot be implemented in 'standard' CMOS processes for improved wireless communication. All of these functions require special manufacturing to optimize the functionality and performance.

Winds are changing

The 3D ASIP conference presentations provided evidence that the industry realizes that 'one process' or 'one architecture' or 'one…' does not, and more importantly cannot, fit for all applications. For decades, "we" have squeezed and compromised as much as we can with homogeneous silicon. "We" are finally hitting economic walls where old, discounted ideas become viable with recent technology and manufacturing advancements. Packaging has become the new frontier for integration solutions, rather than silicon and printed circuit boards. This can be seen with foundries as 'new' competitors in the packaging space. Now we have 'packaging' solutions offered by BOTH silicon foundries as well as OSATs. Each offering different cost/benefit aspects suitable for fragmented market requirements.

The next phase of disaggregation will be the economics and performance (speed, power, etc) required by the fragmented markets. The messages clearly stated during the conference: TSV is not a one solution that ALL must use. Some applications must use TSVs and pay the higher processing/assembly

costs but these markets can support these prices for the performance/power gains required. Other markets with tighter margins are opting for TSV-less complex packaging solutions that still meet their performance/power requirements without the additional costs. If TSV processing ever achieves the cost profiles for these markets, it may not matter.

This new phase will require all to explore long held assumptions about how to develop/design and manufacture their products. This requires exploring new materials and how to best utilize complex packaging that will open up many options to realize their products. Many call this path finding, something that E-System Design understands and supports with Sphinx 3D Path Finder.