A Path Finding Based SI Design Methodology for 3D Integration

Post Paper using 3DPF V3.0

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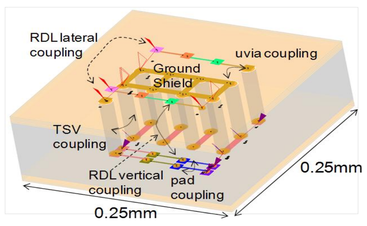
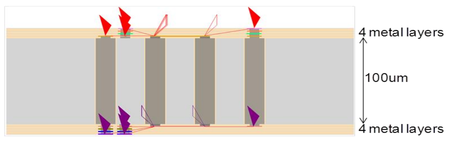
Post Paper Test Cases using V3.0

- Enable analysis with TSV/Planar metal and modeling TSV versus microvia

Example 4: small 0.25mm^2 area silicon interposer

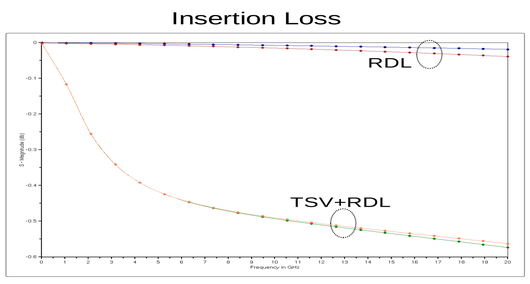


TSV: 20 um Diameter
Oxide: 1um Thickness
uVia: 10 um Diameter
Metal: 1um Thickness
Diele: 2um Thickness
Line: 2um Width

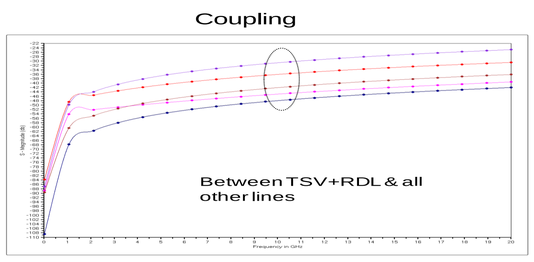


- Analyze considerable coupling in spite of ground shield.
- Ground shield is in the form of grounded TSVs

Responses: small 0.25mm^2 area silicon interposer

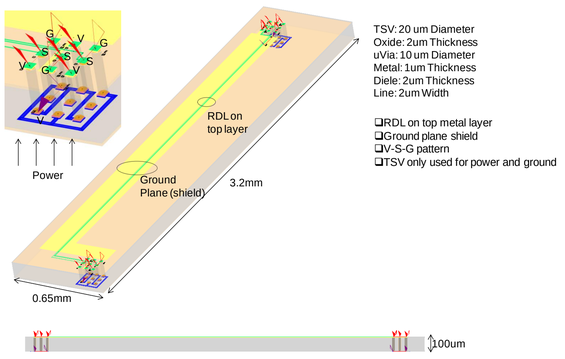


- RDL for this structure has minimal IL degradation since they are routed above or below silicon substrate, while TSV/RDL paths have ~14X worse IL



- In spite of the ground shield using multiple TSVs, the coupling can still be high. In this example the coupling is between -24 to -48 dB.

Example 5: Chip-to-Chip with Interposer (SI/PI analysis)

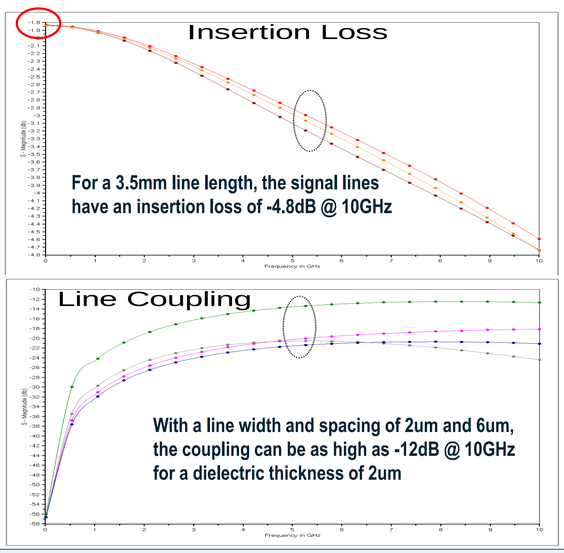


TSV: 20 um Diameter
Oxide: 2um Thickness
uVia: 10 um Diameter
Metal: 1um Thickness
Diele: 2um Thickness
Line: 2um Width

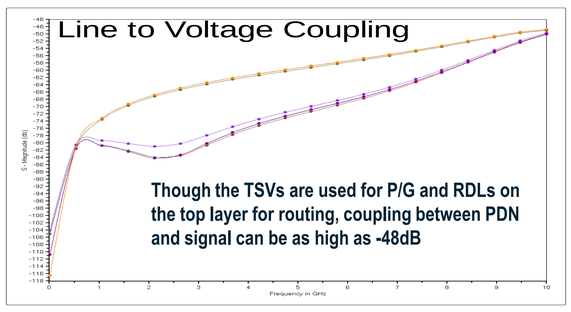
- ❑RDL on top metal layer
- ❑Ground plane shield
- ❑V-S-G pattern
- ❑TSV only used for power and ground

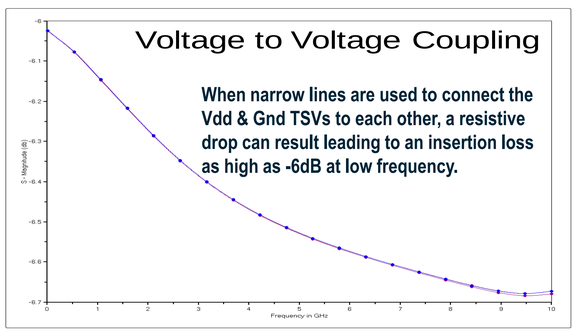
- Analyze the coupling between signal and power distribution

Responses: Chip-to-Chip with Interposer (SI analysis)



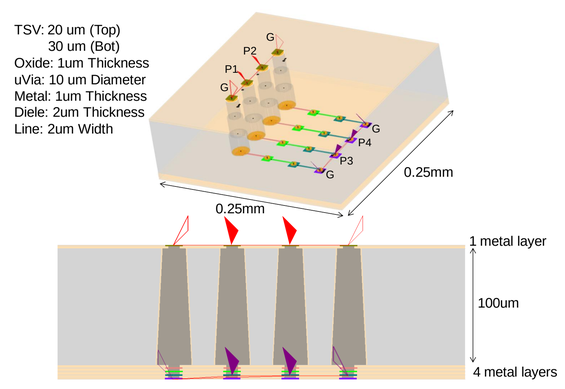
Responses: Chip-to-Chip with Interposer (PI analysis)





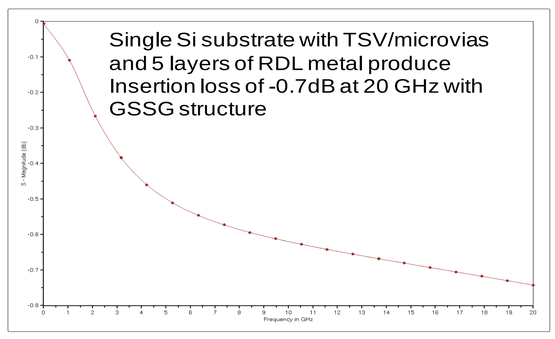
Example 6: Tapered TSV with RDL

TSV: 20 um (Top)
30 um (Bot)
Oxide: 1um Thickness
uVia: 10 um Diameter
Metal: 1um Thickness
Diele: 2um Thickness
Line: 2um Width



- Analyze effect of tapered TSV, RDL, microvias and pads on insertion loss and coupling for a single IC

Responses: Tapered TSV with RDL



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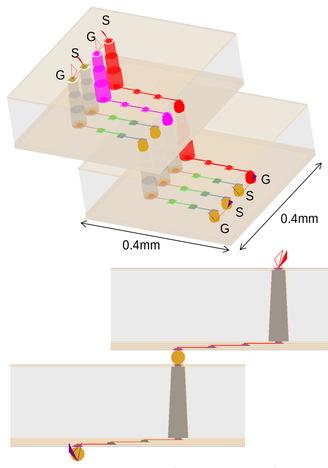
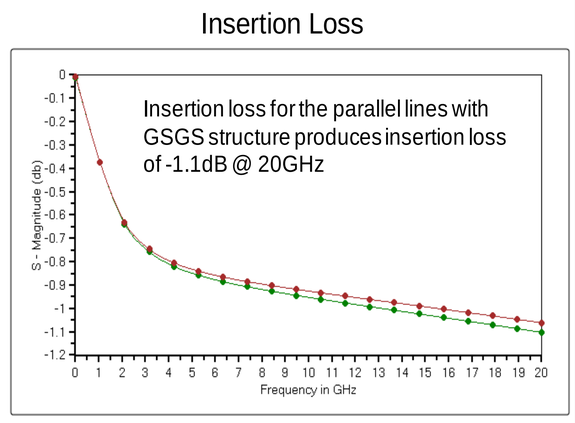
Example 7: Two Chip Stack



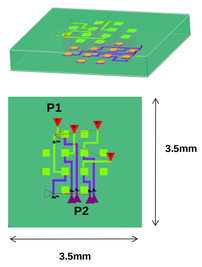
TSV: 20 um diameter (Top)
30 um diameter (Bot)
Oxide: 1um Thickness
uVia: 10 um Diameter
Metal: 1um Thickness
Diele: 2um Thickness
Line: 2um Width
Microbump: 20um diameter

- Analyze impact of stacking 2 IC blocks with TSV and solder bumps: Insertion loss and Xtalk

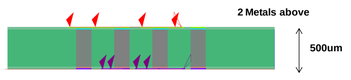
Responses: Two Chip Stack



Example 8: RDL/Via transition

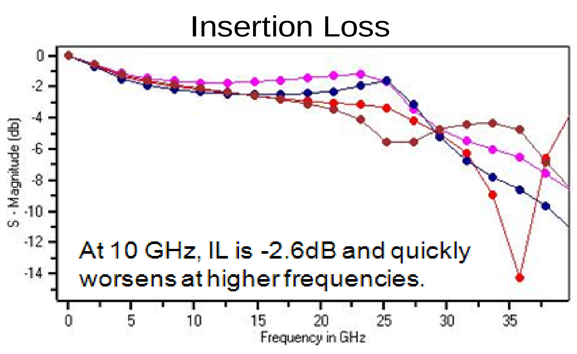


Er	3.9
Metal sigma	5.8e07
Via sigma	5.8e07
Via diam	200um
Via length	500um and 10um
P1 to P2 length	1.37 mm

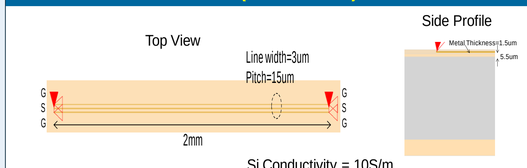


- Analyze: IL and Xtalk for short RDL and via transitions

Responses: RDL/Via transition



Example 9: Unshielded lines in Si Interposer (no TSVs)

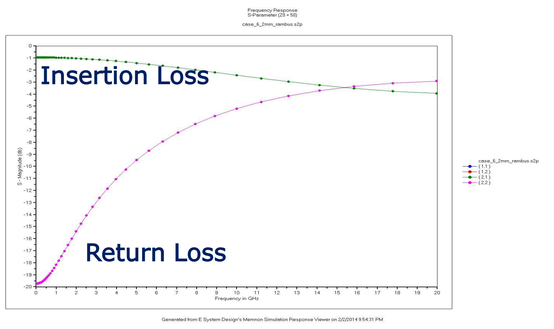


Si Conductivity = 10S/m
SiO_2 = 3.9
Si = 11.9

Ref: 3D Si Interposer Design and Electrical Performance Study, Ming Li, et al, Rambus, DesignCon 2013

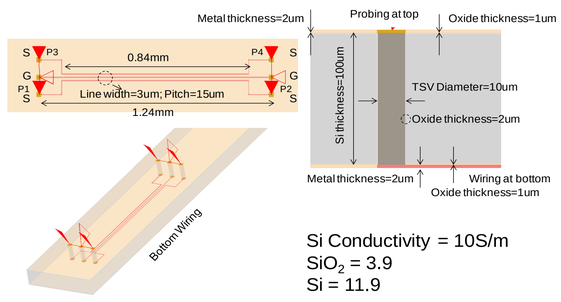
- Analyze: Insertion and Return Losses for GSG structure

Responses: Unshielded lines in Si Interposer (no TSVs)



- Good correlation to presented paper

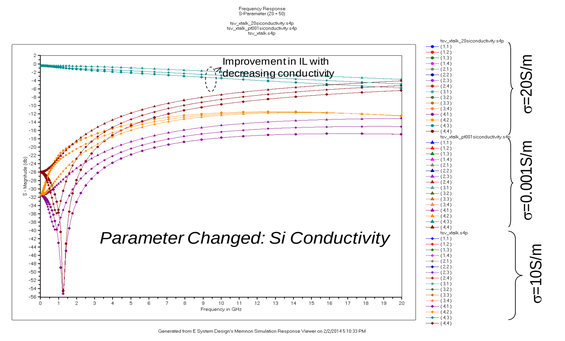
Example 10: Unshielded lines in Si Interposer



Si Conductivity = 10S/m
SiO_2 = 3.9
Si = 11.9

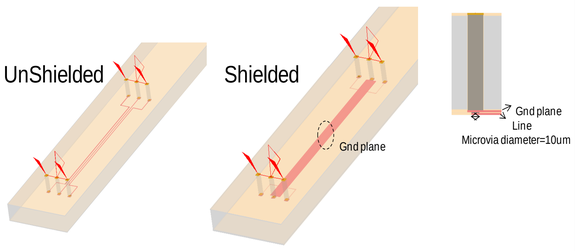
- Analyze: Impact of Si Conductivity on Insertion Loss?

Responses: Unshielded lines in Si Interposer



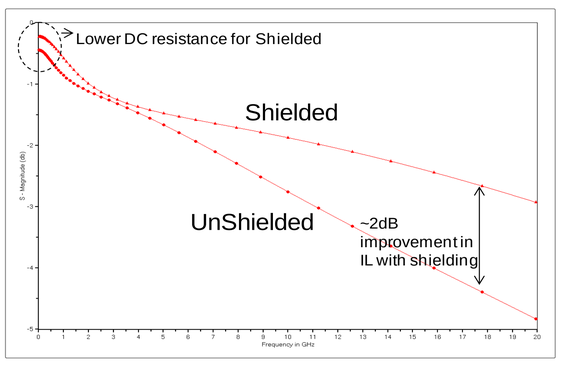
- Improved Insertion Loss with decreasing conductivity

Example 11: Unshielded versus Shielded lines in Si Interposer



- Compare performance of shielded and unshielded lines (SGS) in Si Interposer

Responses: Unshielded versus Shielded lines in Si Interposer



- Shielded improves Insertion Loss by ~2dB
- Lower DC resistance for Shielded