

3D IC Workshop 2010

Organized by : KAIST EECS Tera Lab. / Sponsor : Ministry of Knowledge Economy, KEIT

■ Date : January 14 – 15, 2010

■ Location : KAIST National NanoFab Center, 1F Nano Hall

3D IC Workshop 2010 will be held at KAIST supported by the Ministry of Knowledge Economy.

| Date | January 14, 2010 (Thursday) 9:30 ~ 17:00

January 15, 2010 (Friday) 9:30 ~ 16:40

| Registration | Registration should be made in advance with a first come and first serve basis (up to 100). Please fill in the registration form as shown below and send e-mail to jryu@ee.kaist.ac.kr

Name	Job Title	Organization	E-mail	Mobile Phone

| Registration Deadline | January 11, 2010 (Monday), 17:00 PM

| Workshop Secretary | Jiyun Ryu (jryu@ee.kaist.ac.kr, +82-42-351-9804)

| Website | <http://www.3dic-workshop.org>

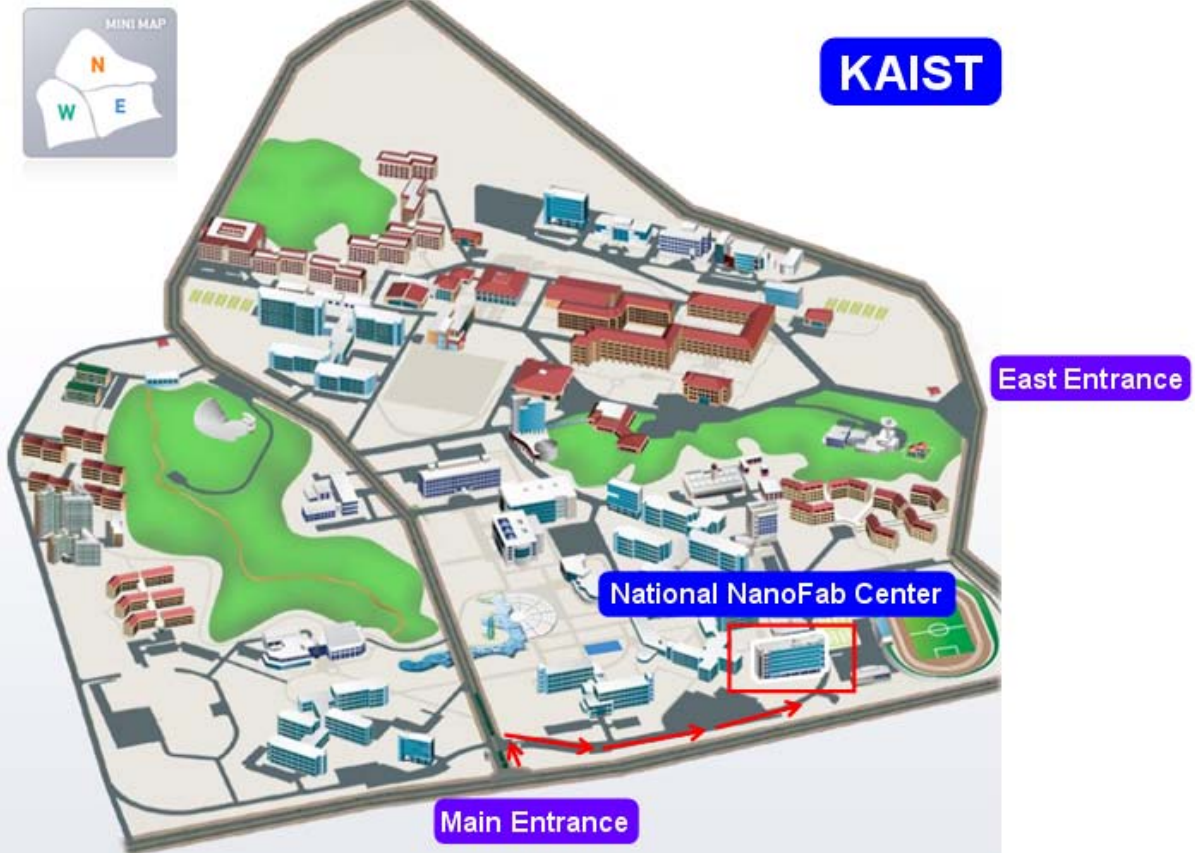
| Location | 1F Nano Hall, KAIST National NanoFab Center, Daejeon, Korea

| Program |

January 14 (Thursday), 2010		
Time	Title	Speaker
09:30 ~ 09:50	Registration	
09:50 ~ 10:00	Opening Speech	Jounggho Kim (KAIST)
10:00 ~ 11:00	3D IC for Energy-aware System Design	Chong Min Kyung (KAIST)
11:00 ~ 12:00	Low Cost Interposer for 3D ICs and Going beyond 3D ICs to 3D systems	Rao Tummala (GaTech, USA)
12:00 ~ 13:30	Lunch	
13:30 ~ 14:00	A Memory Bandwidth Reduction of Graphics Processor by Silicon Interposer Technology	Leesup Kim (KAIST)
14:00 ~ 14:30	3D Stacked Memory Design	Hyungdong Lee (Hynix)
14:30 ~ 15:00	3D Circuit Design with Through-Silicon-Via: Challenges and Opportunities	Sung Kyu Lim (GaTech, USA)
15:00 ~ 15:30	Coffee Break	
15:30 ~ 16:00	Through-Silicon-Via (TSV) Process Evaluation Results at NNFC	Boung Ju Lee (National NanoFab Center)
16:00 ~ 16:30	Novel Bumping and Underfill Materials for 3D Integration	Kwang-Seong Choi (ETRI)
16:30 ~ 17:00	Passive Integrated Si-Interposer for 3D-IC	Jun-Chul Kim (KETI)

January 15 (Friday), 2010		
Time	Title	Speaker
09:30 ~ 10:00	Key Challenges in TSV Commercialization	Taeje Cho (Samsung)
10:00 ~ 10:30	Research Activity on 3D IC in Japan	Masahiro Aoyagi (AIST, Japan)
10:30 ~ 11:00	3D Wafer Level Packaging – Key Processes and Process Integration	Juergen Wolf (IZM, Germany)
11:00 ~ 11:30	Packaging Technology in TSV	ChoonHeung Lee (Amkor)
11:30 ~ 12:00	TSV Structure and Process	Minsuk Suh (Hynix)
12:00 ~ 13:30	Lunch	
13:30 ~ 14:00	TSV – Is it a Wire or a Device? Opportunities for Enhancing System Performance using Through Silicon Vias	Madhavan Swaminathan (GaTech, USA)
14:00 ~ 14:30	Power Delivery Design Challenges for 3D-IC	Heeseok Lee (Samsung)
14:30 ~ 15:00	TSV Design for Power Distribution Network (PDN) on 3D-IC	Jun So Pak (KAIST)
15:00 ~ 15:30	Coffee Break	
15:30 ~ 16:00	TSV Design for Signal Integrity of 3D-IC	Joungho Kim (KAIST)
16:00 ~ 16:30	IC Cooling using Thin Film Thermoelectric Cooler	Shiho Kim (Chungbuk National Univ.)
16:30 ~ 16:40	Closing Remark	Joungho Kim (KAIST)

Map



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