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Are we at an inflection point with silicon scaling and homogeneous ICs?

In the late 1940's, three physicists (Bardeen, Brattain and Shockley) invented the first transistor and were later awarded the Nobel Prize in 1956 (Figure 1). Texas Instruments commercialized the integrate silicon transistor (IC) in 1954 revolutionizing consumer products. The IC invention and commercialization came at a perfect point in history[1,2].

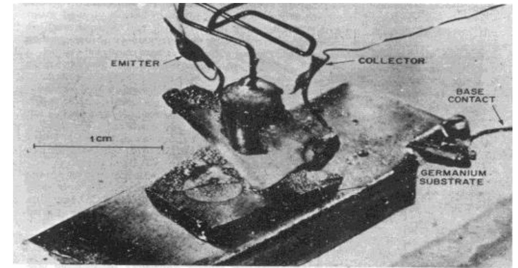


Fig. 1 The first transistor.[1]

During 1950-1970s, the US population grew by 33% (Figure 2), income grew 170% and disposable spending increased 259% (Figure 3). Disposable income was aided by increasing income but also by significant changes to our marginal tax rates. (Figure 4). Consumer demand for better IC based products and their spending $s provided a perfect Petri dish to hone a new technology requiring new processes (silicon, packaging and pcb); supply chains and high tech marketing for future IC based technologies[3,4].

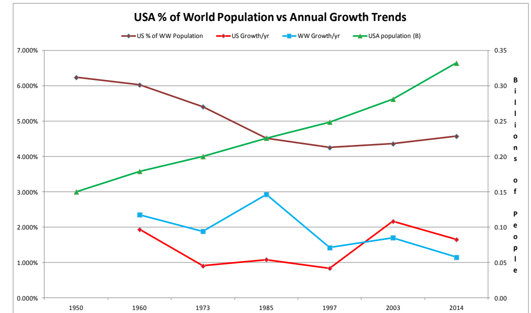


Figure 2

In this period, Moore's Law was 'coined' and quickly drove and guided silicon manufacturers to prove their processing prowess. It also drove product companies and their marketing staffs to harness the guaranteed 2x density, improved performance and less expensive next generation silicon technology within their products. Like an atomic clock, the market expected and received the new capabilities every 18-24 months.

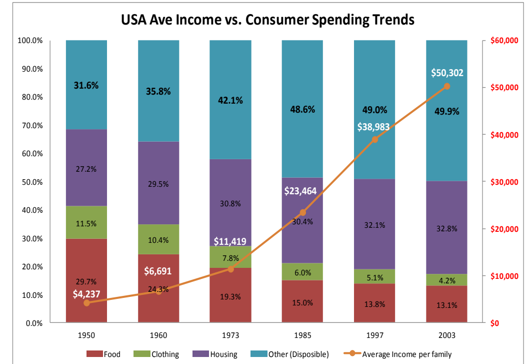


Figure 3

The IC treadmill was at full speed replacing older, larger, slower, higher maintenance products with ICs. As 'they' conquered existing products, new uses from the significant (medical devices), to the trivial (musical greeting cards) were developed to capture the growing disposable income. In the early days, it was cheap to create any type of product to test market acceptance.

Since the 1970's the environment has significantly improved:
US population is over 330 million, annual income is over $50K, disposable spending is approaching 50% and the tax rates continue to fall. In addition, the entire world, 7 billion strong and growing, many wanting to have the latest products. Today's product success benchmark has elevated to a million or more units purchased during a product's life span. Some very well designed and marketed products attain this volume on the initial day of sale (iPhone)!

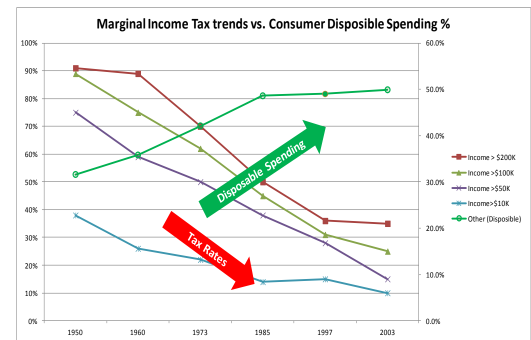


Figure 4

Cracks in the foundation: Inflection omen?

But there were cracks in the foundation starting to appear. More resources, more time and additional physical effects that had to be analyzed and resolved. But engineers are very good at solving these issues that arise with each new generation. One aspect that has not been addressed and is racing out of control is a design's silicon mask costs. Masks allow silicon foundries to build up ICs one layer at a time and define all geometries required for an IC to work. Each physical layer may require 1 or 2 masks. Until the mid 1990's, mask costs were manageable. But as the industry continued to drive toward smaller geometries, 90nm silicon mask costs passed $1M per design[5]. Process engineers had accomplished their goals of producing smaller geometries but this caused an escalation in the required number of masks per layer and the finer geometries increased the cost to create and inspect each mask. Both factors led to a geometric impact on mask costs. Once past the $1M per mask set, the next process' mask prices quickly escalated to $3-4M for a 65nm set. This is just for the masks and does not include other product development costs, wafer/assembly/test manufacturing costs, marketing or sales costs. Quick math: a product with 1 million units of sales that contains one 65 nm integrate circuit will attribute $3-4 dollars to pay back ONLY the mask set expense. FPGA, as a design platform, is one solution but this assumes that your design can be implemented in an FPGA. Many high volume parts still want a dedicated, non-FPGA solution due to per unit costs. Think what the end product's sale's price must be for a decent return on investment (ROI). Economics used to be a friend of silicon linear scaling but we might be at the economic inflection point for linear scaling.

A recent SemiWiki post by Paul McLellan highlights the complexity and change required to continue the silicon scaling[6]:

> "The problem with double patterning is that it is possible to design layouts that cannot be split into two masks…
> To make things worse, this is not a local phenomenon…
> The introduction of both multi-patterning and FinFETs has a **huge impact …**
> …**the entire place and route flow needs to be completely revamped**."

Economics drive the inflection

Will all these technology issues get resolved? Scientists and engineers have conquered most of what they focus on (flying, space, ocean, medical, etc). In time, all of the technical issues can be resolved but what will be the cost to use these 'solutions'? Economics on the product development side (development vs. revenues generated) will cause many product developers to search for alternative solutions or cancel projects that are ROI infeasible.

Moore's Law V1.0 was based upon manufacturing unit learning curves. Each doubling of volume helped decrease the costs to produce the next unit by improving yields. Improving yields allowed designers to create larger die with more transistors and functionality but at a higher cost (at least they could get >0% yield). But this higher cost drove product companies to search for the next generation silicon node that shrunk the die to improve costs: a perfect circular system re-enforcing itself. Figure 5 shows Moore's Law vs. More than Moore

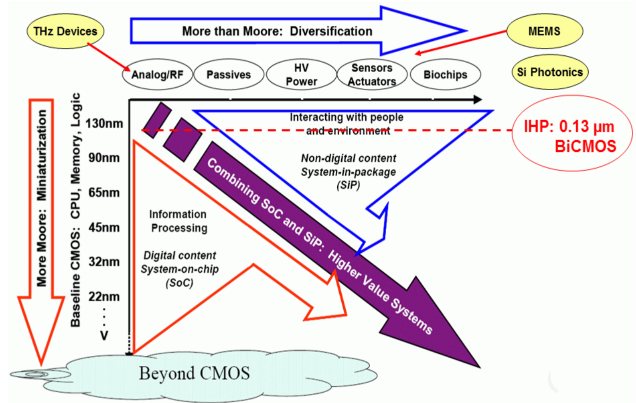


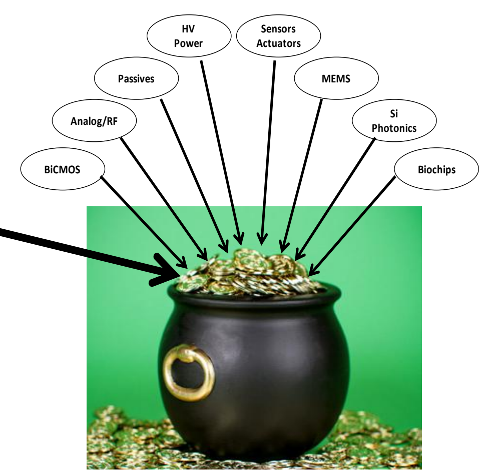
Figure 5

Time for Moore's Law 2.0
(Figure 6: More than Moore modified)

Changing to another solution requires persistence, energy and small successes to gain inertia for Moore's Law 2.0. Packaging becomes the focus on Moore's Law 2.0: 2.5D and 3D allow the mixing and matching of many building blocks into miniaturized systems. Blocks already designed, proven with known histories, costs and suppliers: significantly reducing risks and development costs. Homogeneous silicon will *never* be able to integrate all into a single piece of silicon but must always be available. Too many compromises in the homogeneous processing will reduce the effectiveness of a given function (ie AMS/RF or memory or MEMS or…) and the cost of: tools, masks and processing complexity will quickly cancel any products looking for a positive ROI.

Moore's Law V1.0

Moore's Law V2.0



Homogeneous Silicon Solutions

Heterogeneous Solutions

Figure 6

Maybe not a secret any longer….

Secrets are hard to keep when more and more people start to talk. In recent months, increasing articles and press releases discuss companies that are exploring and/or using 2.5/3D packaging for impressive gains. Many of these efforts have been hidden for either keeping a competitive edge or for fear of public failure. But like many trends, once a trend gains momentum, it is difficult to stop. Moore's Law V1.0 is a perfect example.

If your company is on the Moore's Law V2.0 bandwagon, continue to re-examine old thoughts with a fresh perspective. If your company is not investigating Moore's Law V2.0, you might want to ask why not?

Notes:

1. First transistor picture. http://www.bluekep.com/insanoglunun-en-buyuk-kesfi/ and http://en.wikipedia.org/wiki/History_of_the_transistor.
2. http://en.wikipedia.org/wiki/Texas_Instruments#First_silicon_transistor_and_integrated_circuits.
3. "100 Years of U.S. Consumer Spending", U.S. Departments of Labor and Statistics, May 2006.
4. Annenberg Learner website: http://www.learner.org/courses/envsci/unit/text.php?unit=5&secNum=4.
5. C.R. Helms, Past President & CEO International SEMATECH, "Semiconductor Technology Research, Development, & Manufacturing: Status, Challenges, & Solutions" p16, http://www.nist.gov/pml/div683/conference/upload/Helms_2003.pdf, 2003.
6. Place & Route with FinFETs and Double Patterning, Paul McLellan, Sept 29, 2014, https://www.semiwiki.com/forum/content/3883-place-route-finfets-double-patterning.html.