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Can we learn from the mid 1980's?

Micro vs. Macro cost analysis

Amy Palesko from SavanSys wrote an excellent article (The Cost of 3D ICs) on 3DIncites that focused on the manufacturing cost of TSV enabled devices. No question that these costs are important and will follow a classical manufacturing learning curve. But the real story is at the macro level or system costs using the new technologies.

Introduction of ASIC designs….

Let's rollback the calendar to the mid 1980's when VLSI Technology and LSI Logic created the ASIC. Long before this, any end products required "off the shelf" (standard product) ICs and design them into a printed circuit board (PCB). If a company had the money and time, they could contract for a custom designed IC which was expensive normally only IDMs performed IC design work. In those days, hand drawn schematics and layout, SPICE simulations and manual LayoutVsSchematic (LVS) and crude design rule checks (DRC) were used. Few engineers had the skills to perform these functions so they had to be contracted, if you could find them. This was long before Design Compiler®, Calibre®, VCS®, etc existed[1]. But once tools were developed to help automate these design functions, it opened up IC design to a larger engineering population reducing the costs and risks to IC design.

But these ASIC designs were still **MORE** expensive **AND** riskier than using the available standard products, just because the technical barriers were lowered did not ensure ASIC adoption.

So why were ASICs adopted?

I started to work at VLSI in April 1985. At first, we had small gate array and some standard cell designs that end customers required. These designs were created when no standard products were available in the market. But very quickly, the reason for ASIC design changed to cost reduction solution. VLSI started to get entire system schematics seeing how much we could 'stuff' into as few ASICs as possible. I remember one system that required 11 large PCBoards that we were able to get into a single ASIC die. The end result was an expensive die and several hundred pin ceramic BGA package. If I recall

correctly, the die was 572 mil x 572 mil, the maximum limit for a reticle. To resource this design (people and HW), our team was composed of engineers from several of VLSI Technology Centers[2]. We had to perform physical verification by splitting the die into East and West halves due to size and HW limitations. We had to create behavioral cycle/time accurate models to accelerate simulation from 60 seconds per cycle down to 1 second per cycle. This was a very expensive project to undertake. In addition, the customer ALREADY had this product working with 11 PCBs and countless ICs.

So why did the customer opt for an expensive single chip ASIC?
It was not due to the micro costs of this ASIC: there was no doubt the ASIC was more expensive than any other component in their current system.

It came down to system costs and the performance/power improvements from reducing 11 PCBs into a single chip. Rather than ordering, managing and stocking inventory from multiple suppliers (PCB mfgs, IC providers, etc), they saw a tremendous savings and easier management going to an ASIC design. In many ways, I wish I had the financial before/after for this design. The decision was probably a 'no brainer' once they investigated the system (macro) level costs between the two options and evaluated the single supplier risk (VLSI Technology) versus the many suppliers they had to manage. I seem to recall this ASIC performed as expected.

Why is this relevant?
We have the same situation with complex package integration (2.5/3D). Many of us focus on the 'trees' (micro) and are stuck inside the forest. We need to change our perspective (to macro). Once this is done, complex package integration will become a 'no brainer'.

Notes:

[1] Design Compiler and VCS are trademarked by Synopsys and Calibre is trademarked by Mentor Graphics

[2] On a personal note: VLSI Technology accomplished some fascinating integration feats within our WW Technology Center organization. This is just one example.