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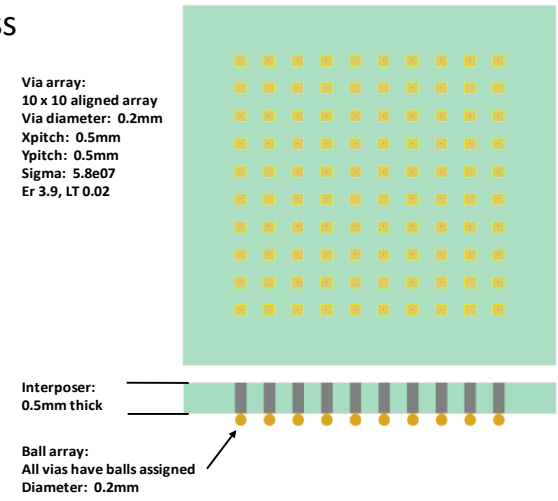
Path Finding and "3DPF"

In the past year, I have written short pieces explaining how Path Finding methodology can proactively help identify viable solutions or reactively identify solutions if something changes during manufacturing. The next few blogs will look at specific examples using a PF tool to help separate the 'wheat from the chaff[1]'.

Signal assignments

When I was designing ASICs/SOCs at VLSI Technology, we normally used SSO 'rules' to help assign signals, power, and ground to die and package pin outs. In older technologies, this normally produced working solutions; but on designs where the 'rules' could not be followed, we manually created SPICE netlists to simulate and validate. Given today's geometries and various implementation choices (silicon versus glass interposers, metal topologies, via array topologies, etc), using Path Finding tools are preferred.



Path Finding helps optimize cost, power, and area during architectural tradeoffs where 100+% improvements can be realized. From my VLSI Tech

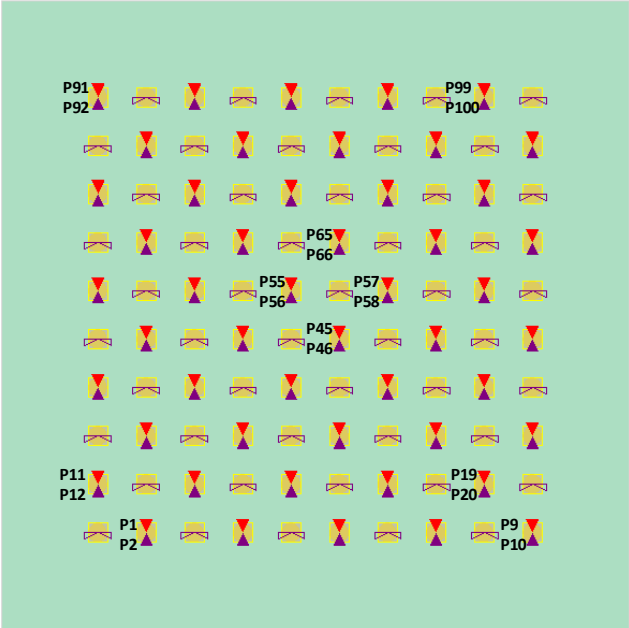
days, once architectural choices are made, only 10-20% improvements can be realized during implementation.

Let's look at a specific example using a SW tool created for accurate and fast Path Finding. For this package test case, a 10x10 via/ball matrix is chosen as shown on right (top and side profile views). [2] No silicon die is included for this experiment.

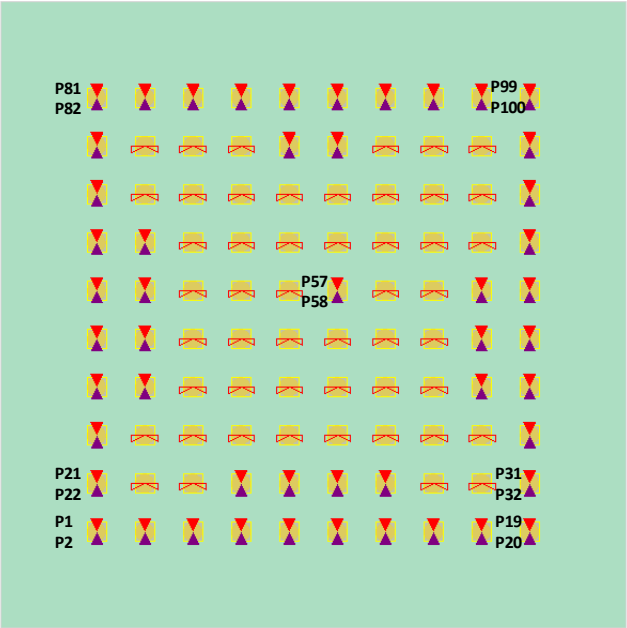
Do signal assignments affect performance and if so, by how much?

To show the impact, I will perform analysis on two different pin assignments that use the same physical structure. Many versions could have been implemented, but this will demonstrate that assignment does matter and should be analyzed before implementation is started. One version will be the classical 'checkerboard' where every other via/ball combination is a signal that is separated by a defined return path. Another version will isolate one via/ball in the center surrounded by return paths, forcing all other signals to be on the periphery. This is shown below where the red triangle denotes a port on the top of a via and the purple triangle represents the port on the bottom of a ball. The 'bow ties' represent common references placed on the top of a via and the bottom of a ball. Fifty via/ball are used for signals while the other fifty via/ball are denoted for return paths resulting in a Touchstone (s100p) file. Simulation was run from 100MHz up to 20GHz[3].

Checkerboard



Non Checkerboard



What do the simulation results show?

We will look at both the Insertion Loss (IL) and the Near End XTalk (NEXT) for both pin assignment options. Each company will set the targeted IL and NEXT that their products must meet to correctly operate in the expected environments. As an example: a cell phone will have different criteria than a medical instrument.

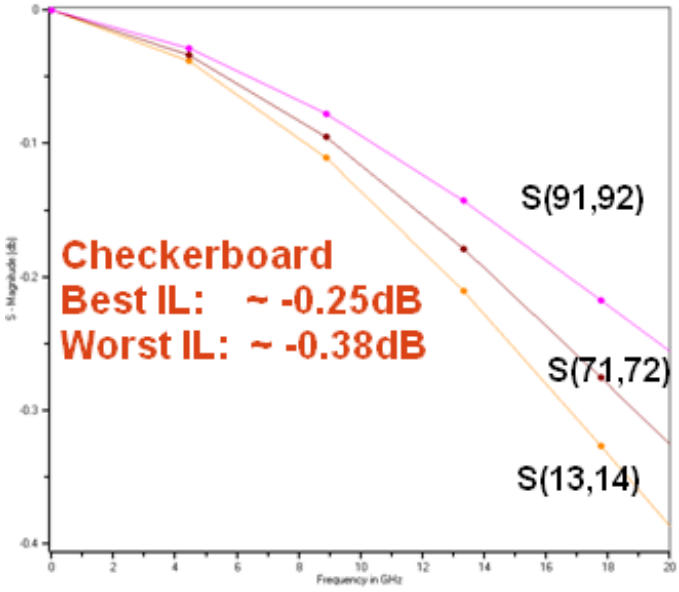
Insertion loss measures between two points how much signal degradation occurs[4]. Whether a signal is transmitted over a cable or on a PCB traces or through a metal trace on a piece of glass or silicon, IL is a key metric to ensure a working system. All signals will have some degradation due to physical implementation and material properties. Normally IL this is analyzed over a frequency range that includes the intended operating frequency range. As the IL increases, the signal received at the far end worsens.

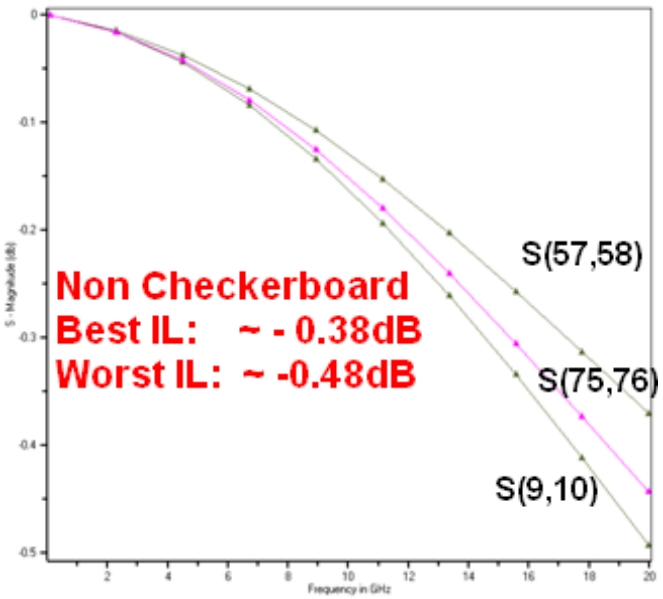
Vin	Vout	dB	% of original Vin
3	3.00	0.00	100%
	2.38	-2.00	79%
	1.89	-4.00	63%
	1.50	-6.00	50%
	1.19	-8.00	40%
	0.95	-10.00	32%

The table shows IL for various combinations of Vout/Vin.

Physical Layer (PHY) blocks used for various interconnect standards (USB, SATA, PCI Ex, ZAUI, etc) are perfect examples. Each interconnect standard has various specifications that must be met to support the standard. Some criteria are: voltage levels, operating frequency range, length of cable, how much signal degradation is acceptable, data throughput, etc. The PHY transmits and receives signals. When receiving, it converts signals into binary 0s and 1s that can be recognized. If a signal degrades outside the criteria and cannot be recognized, data such as movies, songs, emails, etc cannot be sent or received.

Below is the IL for both assignments and you can see that the symmetrical checkerboard improves IL by 0.10dB from best to worst IL at 20GHz. But we need to review NEXT. For the isolation signal (ports 57 & 58), we would expect the Non Checkerboard to provide better noise isolation since it is surrounded by return paths.

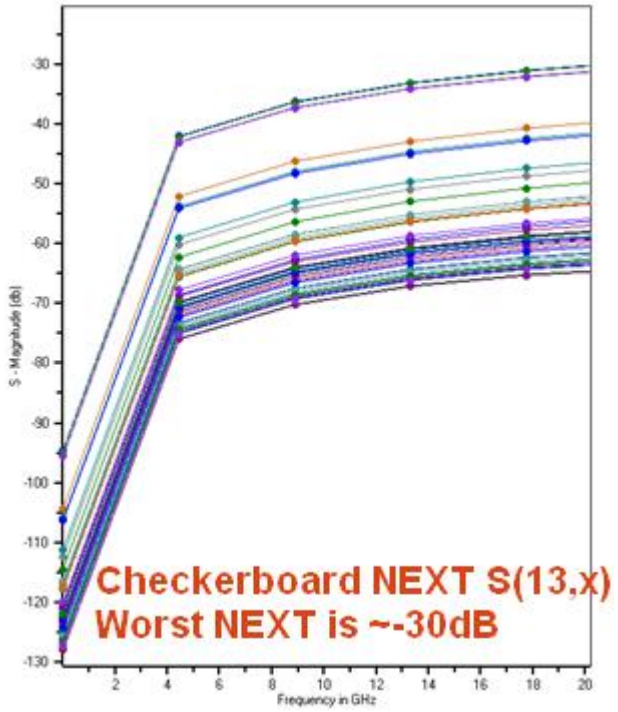


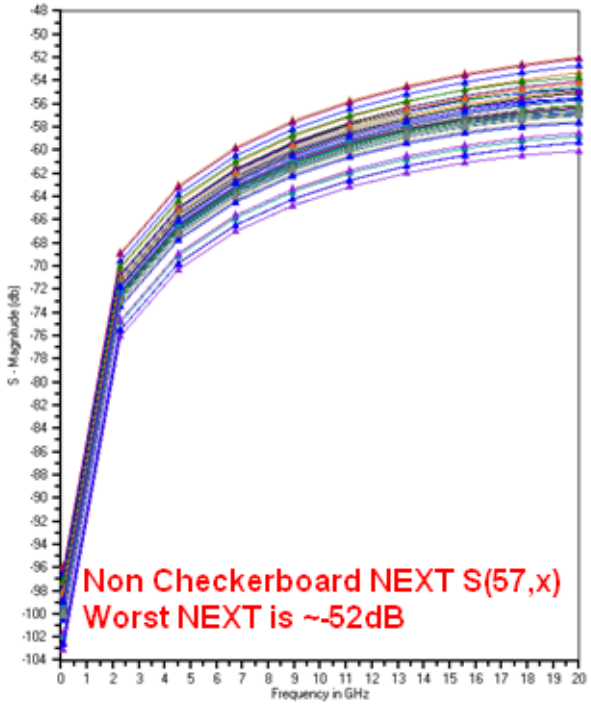


Near End Cross Talk (NEXT) measures the amount of noise between signals[5]. As with IL, this is normally analyzed over a frequency range to ensure functionality. Designers should choose signals that

are critical to their design (clock signals, wide busses, etc) and place ports on the signal lines that are next to each other. Due to near field electric and magnetic coupling, signal lines can lose energy to each other. This can cause the false switching of quiet lines and a reduction in the insertion loss of the driven line. A NEXT between 0 and -20dB can be too noisy while -25dB is approximately 5% coupling between 2 signals.

For the Checkerboard assignment, the NEXT is consistent between S(13,x), S(71,x) and S(91,x). All show a worst-case NEXT approximately -30dB at 20GHz. But if we look at the Non Checkerboard pattern and review the NEXT for the isolated signal with ports 57 and 58, we should expect and do see a dramatic improvement of 22dB better noise immunity (NEXT = -52dB at 20GHz). But how has this assignment altered the NEXT on other signals? Examining Port 9's NEXT, we determine that the worst NEXT is now -18dB at 20GHz, 12dB; poorer than the 'uniform' NEXT achieved with the Checkerboard pin assignment. Although the Non Checkerboard signal assignment has helped with one signal, other signals have been significantly degraded.





What is learned?

As mentioned earlier, each design and its intended environment will influence what IL and NEXT levels are acceptable. If criteria are not met, physical implementation and/or material changes will be required. Some examples:

> Pin assignment does impact performance, and performance can be enhanced by using isolation (keep out zones) to minimize noise.
>
> If a specific pair of via/ball responses were examined, increasing pitch can improve both IL and NEXT, but at the cost of growing the area and cost.
>
> Additional experiments could have also been performed on via/ball pitches to optimize overall IL and NEXT responses.
>
> In addition, vias' lengths/diameters along with balls' diameters and whether underfill is used could be additional Path Finding experiments to help optimize design tradeoffs; all performed before costly implementation is performed.

Before costly choices are made and implemented, it would be wise spending time performing Path Finding.

In future Path Finding, we will look at wire bonds, PDN, RDL topologies, and complex multi tiered structures (package on package).

Notes:

[1] http://dictionary.cambridge.org/us/dictionary/british/separate-the-wheat-from-the-chaff

[2] Creating the basic design required less than 5 minutes to define via and ball profiles, create the array, create a metal layer (pads) between interposer/ball and apply balls.

[3] Upper limit on Sphinx 3DPF simulation engine is 100GHz. These simulations were performed on an Intel i7 CPU 870 @ 2.93GHz with 32G of memory. Four (4) CPUs were used and simulated in several hours. Simulation time can be improved by using more CPUs, larger RAM as well as Solid State

Drives (SSDs). More info at: http://www.e-systemdesign.com/sphinx3DPF.html

[4,5] Professors Swaminathan and Han. Design and Modeling for 3D ICs and Interposers. World Scientific, 2014.