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PDN design, Target Impedance and Path Finding for: IC, Package and PCB

I am fortunate to work with Prof. Swaminathan, our Founder, CTO and inventor of our algorithms. Long ago, as an undergraduate engineering student at University of Illinois focused on integrated circuit (IC) design, I enrolled in the required ElectroMagnetics (EM) course to discover it was all about large antennas. At that time, silicon and EM classes were not synchronized because then-current ICs and their application were largely unaffected by EM. Not having a lot of interest in large antennas, I proceeded to select other electives offered in my engineering track. However, over the past decades since those undergraduate studies, the physics of continual silicon scaling has caused EM to become an ever-increasing design factor in systems that depend on current generation ICs.

In the mid-90's, I taped out my last silicon design. At that time, Synchronous Switching Outputs (SSOs) and signal routing crosstalk just started to impact an IC's "safe operating envelope". The 'tools' we used to manage that impact were guidelines (anecdotal summaries of given process/test circuit performance) and Excel spreadsheets to track silicon device-level simulations and their impact on the IC under design. For critical signals and/or circuits, we would perform Spice simulation to review the voltage/ground noise we could anticipate. The terms 'Power Distribution Network', and, 'Target Impedance' were not used during the design because the EM problems while computationally difficult, were straight-forward to manage using the process node's best practices.

Today, it's a completely different story. On-time delivery of operational ICs and the associated end-user products require design teams to spend significant effort planning, adhering to, and verifying an effective EM strategy that starts with collaboration on the IC's and system's Power Distribution Network (PDN).

This blog will show how Path Finding (methodology and tool) can help accelerate early PDN planning. For deeper SI/PI information, please visit E-SystemDesign website and watch Prof. Swaminathan's SI/PI video series.

Power Distribution Networks[2]

A PDN is 'simply' how Power and Ground are supplied throughout a design. It can have several sub-systems such as Integrated Circuit (IC), Package and Printed Circuit Board (PCB). PDN's typically are a repeated structure that can be decomposed into a leaf cell that is arrayed. Remember, we want consistent PDN performance across the design. Each sub-system works at different frequencies and each PDN must account for this. The IC PDN will have the fastest operating frequencies and signal switching while the PCB PDN will have mostly slower signaling.

To improve how PDN's perform, designers will specify Power Supplies, Voltage Regulator Modules, Capacitors, Resistors and Inductors to improve the PDN sub-system's performance. Poorly designed PDN's will cause higher power dissipation (less battery life), increased noise throughout the system potentially causing functional failures, slower performance due to slower signal rise and fall times, etc. But to determine whether a PDN is good or not it must be analyzed over the operating frequency range. A single frequency is inadequate in today's systems that have a wide range of signal frequencies. If we were solely working in Direct Current (DC), Ohm's Law would allow us to capture the PDN's resistance and help reduce the power (Power = Current^2 x Resistance). Reducing the operating Voltage or the Current required is difficult so the focus is on reducing the Resistance (denoted as 'R') therefore reducing the Power dissipated. But since we are using Alternating Current (AC) we must deal with a frequency range and rather than Resistance, we focus on Impedance (denoted as 'Z') as our metric to guide our design efforts. In AC analysis, as with DC/Resistance, lowering the Impedance as low as economically feasible is the goal to reducing many issues mentioned earlier.

Target Impedance[2]

Impedance is a function of capacitance, resistance and inductance and varies over frequency. Therefore, lowering the impedance requires a target impedance and determining where anti-resonances occur. Anti-resonances are frequencies where the Impedance (Z) is significantly higher than other frequencies' Impedance (Z) levels (Figure 2a shows an example).

The definition of Target Impedance (Z_T) is: $Z_T = (V_{DD} \text{ X ripple})/(50\% \text{ X } I_{max})$

V_{DD} is the supply voltage and 'ripple' is the percentage of supply voltage (V_{DD}) that the transistors can tolerate without failure. I_{max} is calculated from the Power and Voltage. '50%' is a fudge factor representing an average current. Prof. Swaminathan's first video in his SI/PI video series shows how critical the PDN's impact on a chip's performance. Over the past few

decades, supply voltages have been reduced from 5 volts down to 0.8 volts (or lower). This was required due physical damage high voltages caused to silicon transistors. One upside of lower supply voltages is reduced power dissipation but a downside is the reduced supply voltage tolerance levels making a designer's job more difficult.

When anti-resonances impedances are ABOVE the Targeted Impedance (Z) are identified, the designer will need to add capacitors to lower the impedance at that frequency. If the anti-resonance impedances are below the Targeted Impedance (Z) value, nothing needs to be done saving the capacitor's cost along with the manufacturing costs (inventory, handling, yield loss, etc). If capacitors were added in this situation, this is over design without affecting the PDN's performance. Many books and articles have been written how to design and reduce anti-resonance impedance[2].

How can Path Finding help early PDN design using Target Impedance?

As discussed in previous 3DIncite blogs, Path Finding allows designers to quickly test various ideas to help separate the viable from the inane. The same can be applied to PDN test cases where various PDN architectures are implemented: various metal layers and topologies, vias diameters and locations, PDN size, etc. Instead of reviewing Insertion Loss (IL), Return Loss (RL), Near and Far End Cross talk (NEXT and FEXT, respectively), we will review Self and Transfer Impedances. Noise between different Power Planes will be discussed in a future blog. In previous blogs, structures were created, ported and simulated: PDN is a similar process. The port placement will be slightly different due to PDN analysis and what responses are reviewed will differ (Z and magnitude).

Let's analyze a test case to show what can be accomplished.

The test case is a simple lattice PDN with 2 layers of metal and uvias connecting the PDN between the layers. The VDD nets are 20um wide while the GND nets are 40um wide, the total leaf cell is 0.5mm x 0.5mm. uvias connect the metal2 (blue) to metal1 (pink) and have a diameter of 0.01mm (Figure 1b). For each location that VDD metal2 crosses above VDD metal1, a uvia is added. A similar uvia structure is used for the GND crossovers. A total of 50 uvias are used (25 VDD and 25 GND) to connect metal2 to metal1. Notice that the leaf cell has two TSVs (0.01mm diameter with 0.002 Oxide liner) which allow the PDN to be powered from the bottom of the 100um thick silicon substrate (Figure 1a). Leaf cell porting is divided into two types of ports. The first type is periphery ports that are used to connect leaf cells to neighbor leaf cells. In this case, all ports on the North, South, East and West boundaries are periphery ports (10 ports per side, 40 total). The second port type identifies additional locations we may want to monitor at the PDN arrayed level. In this case, four additional ports were added (2 near the center and 2 near the bottom left-hand corner).

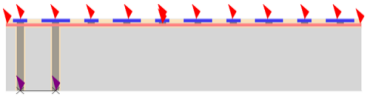

Figure 1a Leaf Cell Profile

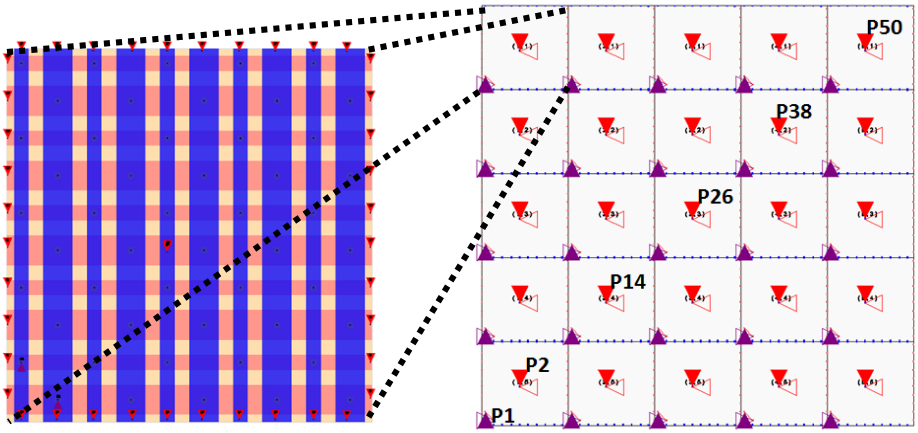

Figure 1b Leaf Cell

Figure 1c PDN array (5x5 leaf cells)

Figure 1c shows the PDN comprised of 25 leaf cells in a 5x5 configuration. Any rectangular PDN structure can be created by varying the PDN's MxN array settings. A single VDD net and GND net are formed for the entire PDN. For this design we will look at the Self Impedance and the Transfer Impedance between different locations. On the PDN array, 50 ports have been placed and 6 are specifically shown (P1, P2, P14, P26, P38 and P50). Port P1 is placed on the bottom of the TSVs while the other 5 ports are located on the diagonal leaf cell centers. The PDN ports will allow us to capture responses for the entire PDN array. Notice that PDN ports match up with the 4 additional ports mentioned in the previous sections. This test case was easily constructed and analyzed in the same tool: Sphinx 3DPF[3]. This is just one test case but with Path Finding, other test structures might be created that vary metal/via topologies, material properties, etc to identify the affects of these changes and whether a better PDN can be designed. On my machine, an Intel i7 870 with 4 CPUs @ 2.93GHz and 32G of memory, this required under 10 minutes to simulate.

What do the simulation results show?

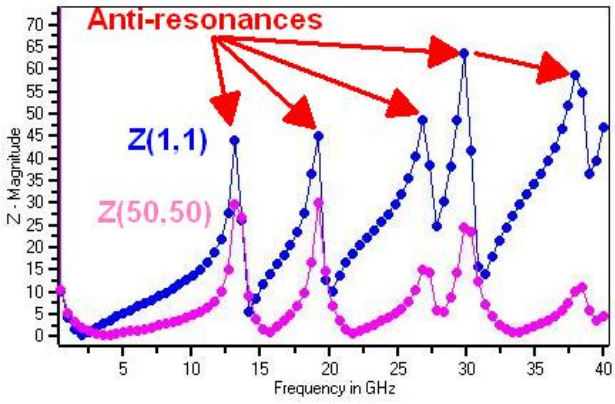

Figure 2a Self Impedance

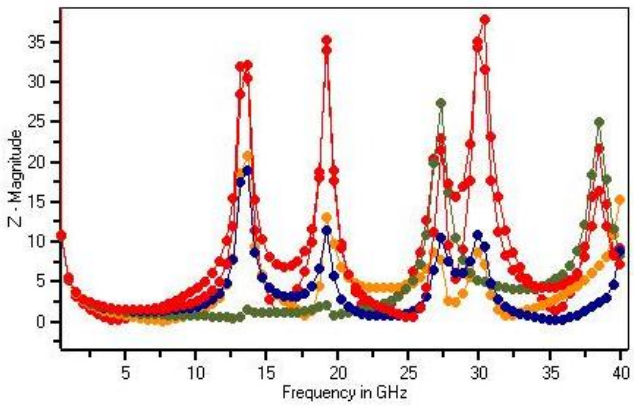

Figure 2b Transfer Impedance

With this information, a designer can determine if this leaf cell is sufficient for their design and understands the anti-resonance frequencies to address to improve their overall PDN Impedance profile. If the user wants to perform Time Domain analysis, the entire 5x5 arrayed PDN's Touchstone file can be converted to a Spice macro model allowing the user to add sources and sinks where top level PDN ports have been placed. This compact model can be combined with other PDN models (ie Package, Interposer and/or PCB) to simulate their entire system level PDN.

Want additional info?

Technical papers that discuss the Engine behind "3DPF" will be presented at EPEPS (October: San Jose, USA) and EDAPS (December: Seoul, Korea). Two other application related papers will be presented at Zuken Japan (October: Tokyo, Japan) and 3D ASIP (December: San Francisco, USA) conferences.

Notes:

[1] I have talked with a few University of Illinois professors at EPEPS Conferences and the EM classes are no longer only focused on large antennas.

[2] Professors Swaminathan and Engin. Power Integrity Modeling and Design for Semiconductors and Systems. Prentice Hall 2008.

[3] This is using Sphinx 3D Path Finder ("3DPF") which is sold and supported by E-SD. In addition, patents are granted and pending.