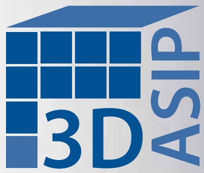

3D Architectures for Semiconductor Integration and Packaging

The Technology and Market Landscape for Device and Systems Integration and Interconnect

3D ASIP December 10-12, 2014, Burlingame, California

Now celebrating its 11th year, the longest running conference series on this topic – **3D ASIP** – continues to be an outstanding venue to meet with leaders from around the world to learn and discuss the latest technology and market insights into 2.5/3D device and systems integration and packaging. The conference format offers attendees a platform to gain the latest information from invited speakers on technology progress and industry trends that define this sector today and tomorrow. Along with the invited presentations, the full program includes two preconference symposiums, and various networking functions with opportunities to meet and talk with fellow industry leaders.

Most industry observers believe growing 2.5/3D technology adoption is imminent, offering the best longer-term solution to the industry challenges in size, power, and performance; however the timetable has proven fluid, with most market forecasts to date being perhaps overly optimistic. Today many experts suggest that the technology is, in fact, ready for large-scale commercial manufacturing adoption, and that the tipping point in driving down costs will be the volume manufacturing of stacked memory with logic. Others, though, point to the enabling features of 2.5/3D integration and packaging approaches driving development of a range of next-generation systems, from integrated photonics to MEMS and sensor systems supporting the emerging IoT industry, and that establishing design infrastructure is key. While these and other questions remain, the market opportunities are clearly significant.

The key objective of the 2014 conference is to continue to provide a unique meeting point, dedicated to serving the needs of the entire 2.5/3D ecosystem, from technology developers to equipment and materials suppliers to designers, manufacturers, and end users. The conference and presentation format give speakers the freedom to share the very latest insights and information. With invited speakers and participants from leading companies and organizations around the world, the conference aims to provide information critical to planning ongoing and future business and technical efforts impacted by 2.5/3D developments and opportunities.

Speakers from

Apache Design, an ANSYS subsidiary
Atrenta
Cadence
CEA-Leti
eda2asic
eSystem Design
EV Group
Fraunhofer Institute for Integrated Circuits
General Electric
Georgia Institute of Technology
GLOBALFOUNDRIES
IBM T. J. Watson Research
Invensas
Mentor Graphics
Microelectronic Consultants of NC
Micron Technology
MonolithIC 3D
NANIUM
Novati Technologies
NVIDIA
Qualcomm
Rambus
RTI International
SavanSys Solutions
Si2
Synopsys
TechSearch International
Tohoku University/GINTI
UC Santa Barbara
Unimicron
Xilinx
Yole Développement

TWO Preconference Symposiums ...

10 Dec 2014 | 8:30 a.m. – 12:30 p.m.
2.5/3D-IC Design Tools and Flows

10 Dec 2014 | 1:30 – 5:00 p.m.
3D Integration: 3D Process Technology

Symposium registrations include bonus publications and handouts

www.3dasip.org

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Two Preconference Symposiums

2.5/3D-IC Design Tools and Flows

10 Dec 2014 | 8:30 a.m. – 12:30 p.m.

Within the last several years many IC design teams developed, in cooperation with their supply chain partners, about 100 evaluation units, to define design flows and better understand the benefits of stacking dice on interposers or vertically. Likewise the manufacturers used these evaluation units to hone their manufacturing flows and drive cost-reductions. Now both sides are ready to develop designs for volume production and need EDA tools to walk the fine line between costly over-design and unreliable under-design.

In this session EDA vendors and IC manufacturers outline their cooperation to provide system and IC designers the means to implement and verify their ideas in 2.5/3D ICs.

Symposium Chair: Herb Reiter, President, *eda2asic Consulting*
Bill Martin, President, *eSystem Design*
Zafer Kutlu, PMTS Packaging Engineer, *GLOBALFOUNDRIES*
Brandon Wang, Group Director, Chief Strategy Office, *Cadence*
Norman Chang, VP Design Solutions, *Apache Design, an ANSYS subsidiary*
John Ferguson, Ron Press, John Park, Marketing & Methodology, *Mentor Graphics*
Ming Li, Sr. Principal Engineer, *Rambus*
Durodami Lisk, Principal Engineer/Manager, *Qualcomm*
Jerry Frenkil, Low-power Consultant, *Si2*

BONUS: *2.5/3D-IC Design Guide 2014*

3D Integration: 3D Process Technology

10 Dec 2014 | 1:30 – 5:00 p.m.

With the 2014 announcements of TSV-based memory stacks from Micron, Hynix, and Samsung the Era of 3DIC has officially begun. RTI International's 3D ASIP preconference symposium will take a quick look at the current status of the 3D marketplace and then a more detailed look at the status of 3D TSV-based processing technology.

Symposium Chair: Phil Garrou, IEEE Fellow and Consultant, *Microelectronic Consultants of NC*

The Status of the 2.5/3DIC Marketplace

Phil Garrou, IEEE Fellow and Consultant, *Microelectronic Consultants of NC*

TSV Formation: Drilling and Filling

Dean Malta, 3D Integration and Advanced Packaging, *RTI International*

Temporary Bonding and Via Reveal

Severine Cheramy, 3DIC Laboratory Manager, *CEA-Leti*

Assembly

Laura Mirkarimi, VP of Design, Analysis and Reliability, *Invensas*

BONUS: *Handbook of 3D Integration: 3D Process Technology, Volume 3*

10 December

8:30 – 12:30 p.m. Preconference Symposium
2.5/3D – IC Design Tools and Flows

1:30 – 5:00 p.m. Preconference Symposium
3D Integration: 3D Process Technology

6:00 – 8:00 p.m. Registration and Welcome Reception
Sponsored By: Tezzaron

11 December

6:45 – 8:00 a.m. Registration and Continental Breakfast
Sponsored By: SUSS MicroTec

8:00 a.m. Welcome and Opening Comments
Matthew Mecray, Conference Director, *RTI International*

Conference Cochairs:
Phil Garrou, IEEE Fellow and Consultant, *Microelectronic Consultants of NC*
Mark Scannell, Director Business Development, *CEA-Leti*

Keynote Session

A Design Ecosystem for Internet of Things, How 3D IC Standards will Enable a New Growth Paradigm

Steve Schulz, President and CEO, *Si2 - Silicon Integration Initiative*

- 3D IC: a long path toward adoption
- Internet of Things, a catalyst for design methodology change
- Mitigating risk and optimizing designs: heterogenous 3D IC stacks play a key role
- Enabling a maker community for the semiconductor players
- Design standards: providing the structure to enable the coming IoT disruption

2.5D and 3D Memory Solutions: An Overview and Outlook

Robert Sturgill, Director, *Hybrid Memory Cube Solutions Micron Technology*

- The landscape today for 2.5D/3D ICs
- Solution comparison
- Challenges and considerations
- What's ahead and requirements for success

UltraScale 3D FPGA

Xin Wu, VP Silicon Technology, *Xilinx*

- Moore's Law is more challenging and more expensive today
- Expanding the capability of integration via 3D-ICs
- 3D-IC product considerations
- Xilinx' approaches
- Next generation of 3D FPGA

9:45 – 10:15 a.m. Break
Sponsored By: Invensas

IoT, Memory and More than Moore

The Internet of Things: From Hardware to Cloud and Data Processing through Heterogeneous Integration

Rozalia Beica, CTO, *Yole Développement*

- IoT market drivers and applications
- Market structure and forecast
- Technology trends and IoT evolution
- Heterogeneous integration
- Technology challenges

Will Industrial Internet Drive Next Semiconductor Revolution?

Samta Bansal, Product Marketing Leader, *General Electric*

- IOT: Shades of gray
- What is industrial Internet?
- Lens into some current and future applications and technology Asks
- What does that mean to semiconductor world?

More-than-Moore as a Disruptive Force in the Electronics Packaging Industry

Dave Anderson, President and CEO, *Novati Technologies*

- MtM enabling customer solutions
- Heterogeneous material integration
- Converting novel ideas into reality

Next Generation 3D and 2.5D Stacked Memory Systems

Alok Gupta, Principal Engineer, *NVIDIA*

- Motivation
- Future memory technologies
- 2.5D and 3D memory systems
- System design challenges
- Conclusion and future work

12:15 – 1:30 p.m. Lunch

Perspectives on Manufacturing and Costs

The Last Mile: Moving 3D IC into HVM

E. Jan Vardaman, President, *TechSearch International*

- Today's application moving into HVM
- Planned applications
- Co-existing with an interposer solution
- Technical challenges still requiring attention
- Market outlook

Addressing Challenges in 2.5D and 3D IC Assembly

Sitaram Arkalgud, VP 3D Portfolio & Products, *Invensas*

- Critical stacking challenges
- Assessment of assembly options
- Manufacturability
- Innovations

Will the Cost of 3D ICs Ever Be Low Enough for High Volume Products?

Chet Palesko, President, *SavanSys Solutions*

- 3D IC cost drivers
- Barriers to adoption in high volume products
- Future high volume product requirements - will 3D be required?

3:00 – 3:30 p.m. Break
Sponsored By: Invensas

Panel Session

How Can We Further Strengthen the Foundation for 2.5/3D-IC Pathfinding?

A decade ago Floorplanning became a very important design step. Today's System and IC Designers need more powerful tools and a broader range of inputs to partition complex designs and determine best possible alternatives for implementing multi-dice designs in single packages. Several industry segments and academia have been working together for a few years to develop data formats, tools and methods to meet these needs. Experts from these segments will outline status, discuss how best to proceed and answer questions from the audience.

Moderator – Herb Reiter, President, *eda2asic Consulting*
Durodami Lisk, Principle Engineer/Manager, *Qualcomm*
Ravi Varadarajan, Fellow, *Atrenta*
Markus Wimplinger, Director Technology and IP, *EV Group*
Yuan Xie, Professor, *UC Santa Barbara*

Design Analysis and Modeling – Signal Integrity, Thermal and Power Considerations

Performing 3D-IC Design Trade-off with Fast Power/Thermal/Signal Integrity Analyses for Early Design Stages

Norman Chang, VP and Sr. Product Strategist, *Apache Design, an ANSYS subsidiary*

- Introduction on the need of PI/TI/SI analyses for early design stages
- Fast P/G/TSV network generation in 3D-IC
- Efficient TSV extraction considering silicon loss in Power Integrity Analysis
- Power-thermal co-simulation with what-if design parameters
- Early SSO analysis and summary

TCAD Modeling for Stress Management in 3D IC Packages

Terry Ma, Vice President Engineering, *Synopsys*

- Thermal mismatch stresses in 3D IC
- Modeling stress evolution with TCAD
- Analyzing stress effects on performance and reliability
- Modeling chip packaging interactions
- Stress management in 3D IC technology integration and design

6:00 –8:00 p.m. Evening Reception
Sponsored By: EV Group

12 December

6:45 – 8:00 a.m. Registration and Continental Breakfast

The World in 2.5D – Interposers

Status of Manufacturing and Design of 2.5D Package Technology

Zafer Kutlu, PMTS - Packaging Technology, *GLOBALFOUNDRIES*

- 2.5D technologies and application space
- Silicon interposer design flow
- Silicon interposer key processes and status
- Design considerations for 2.5D integration

The Next Generation Fan-Out WLP Technology eWLB – High Density WLSiP

Steffen Kroehnert, Director of Technology, *NANIUM*

- Thin active interposer, multiple actives and passives embedding
- Smaller line/space for higher I/O count

3D From the Perspective of a Research Institute

Mark Scannell, Director Business Development, *CEA-Leti*

- 'Active interposers' with fine pitch TSV's for high-performance computing
- TSV-free 3D enabling the Internet of Things

Si Interposers - Making the Move from PWB to Si

John Lannon, Director, Microsystem Integration and Packaging, *RTI International*

- System level design considerations
- Interposer design and process options from IC foundries
- Interposer design and process options from post-CMOS companies

Advance Substrate Development for Semiconductor Integration

Dyi-Chung Hu, Sr. Advisor, *Unimicron*

- Laminate substrate
- Fine line
- Glass substrate
- Interposer
- PoP

10:30 – 11:00 a.m. Break

Monolithic 3D Integration – An Emerging Reality?

M3D a Disruptive Approach for Further Scaling

Hughes Metras, VP Strategic Partnerships, North America, *CEA-Leti*

- Ultra high density transistor stacking
- Low temperature process and tools requirements
- 3D design tools and methodologies

Fusion Bonding for Next Generation 3D ICs

Thomas Urhmann, Director of Business Development, *EV Group*

- Hybrid wafer bonding and monolithic integration
- New devices with bond alignment below 200nm (3σ)
- Fusion bonding for heterogeneous integration and chip stacking
- Fusion bonding of carrier mounted ultra thin wafers
- Control of wafer deformation during bonding

Precision Bonders – A Game Changer for Monolithic 3D

Zvi Or-Bach, CEO, *MonolithIC 3D*

- Introduction to monolithic 3D
- Known process flows
- The game change - monolithic 3D for every fab
- Taking care of the heat
- The monolithic 3D unparalleled advantage

12:30 – 1:45 p.m. Lunch

2.5/3D Systems – Bringing it all Together

Quick Prototyping of Heterogeneous 3D/2.5D Integrated Devices for Intelligent Microsystems

Mitsumasa Koyanagi, Professor/Director, *Tohoku University/GINTI*

- Heterogeneous 3D/2.5D integration for intelligent microsystems
- Heterogeneous 3D/2.5D integration technology for quick prototyping
- Intelligent microsystem using 3D-stacked stereo vision image sensor
- Intelligent microsystem using 3D-stacked multi-core processor with self-test and self-repair function

Technology, Simulation and Design for 3D Integrated Heterogeneous Sensor Systems

Peter Schneider, Department Head, Heterogeneous Systems, *Fraunhofer Institute for Integrated Circuits*

- Introduction
- Technology platform for heterogeneous sensor integration
- Design challenges
- Heterogeneous integration in sensing applications and medical implants
- Summary and outlook

Large and Scalable Silicon Interconnection Platform using Electrical, Photonic, and Thermal Interconnect Networks

Muhannad Bakir, Associate Professor, ON Semiconductor Junior Professor, *Georgia Institute of Technology*

- Interposer bridging
- Dense electrical interconnects using flexible joints
- Self-alignment of dice and interposer
- Electrical and photonics interconnect networks
- Advanced cooling in interposer

Embedded Two Phase Fluid Cooling for 3D

Michael Gaynes, Sr. Technical Staff Member, *IBM TJ Watson Research*

- Design
- Fabrication
- Modeling
- Experimental study

3:45 pm Closing Comments

Hotel Information

The Hyatt Regency San Francisco Airport Hotel is located 2 miles from the San Francisco International Airport and 14 miles south of San Francisco. Make your reservations by November 24 to receive the conference rate.

Call 650.347.1234 and mention you are attending RTI's 3D ASIP conference to receive the special room rate, or visit the conference website, **www.3dasip.org**, and click on the hotel link to make your reservations online.

Register online at www.3dasip.org

Preconference Symposiums—Register to attend one or both of these technical sessions covering 3D IC design and processing. Registration includes, the selected session(s) and proceedings, and special bonus handouts as noted below.

Wednesday Morning Session
2.5/3D-IC Design Tools and Flows
Moderated by Herb Reiter
BONUS: 2.5/3D-IC Design Guide 2014

Wednesday Afternoon Session
3D Integration: 3D Process Technology
Moderated by Phil Garrou
BONUS: Handbook of 3D Integration: 3D Process Technology, Volume 3

	Corporate	Univ/Gov
One Symposium Only	$ 499	$ 499
Both Symposiums Only	$ 749	$ 749
Conference Only	$1249	$ 849
Conference and One Symposium	$1649	$1249
Conference and Both Symposiums	$1899	$1499
Proceedings	$ 499	$ 499

Conference fees include continental breakfasts, lunches, receptions, handouts, and proceedings. Symposium fees include refreshments, handouts, symposium proceedings, and bonus publications.

RTI International c/o YCC
2520 Independence Blvd., Suite 201
Wilmington, NC 28412

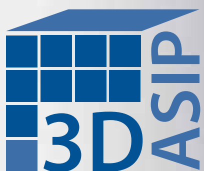
Exhibits and Sponsorships

EXHIBITS: Showcase your products or services by reserving table-top exhibit space. The exhibit area is located near the main conference room.

Exhibit Table (registered to attend)	$1000
Exhibit Table	$1500

SPONSORSHIPS: Increase your company and product exposure at this conference and in the industry as a 2014 3D Architectures for Semiconductor Integration and Packaging sponsor. Visit the conference website **www.3dasip.org**, or contact Karen Dobkin at 910.452.0006, or **karen@teamycc.com** for details.

RTI International is a trade name of Research Triangle Institute.



3D Architectures for Semiconductor Integration and Packaging

3D ASIP December 10-12, 2014, Burlingame, California

MAKE PLANS TO ATTEND TODAY ...

This conference provides a unique perspective of the techno-business aspects of the emerging commercial opportunity offered by 3D integration and packaging—combining technology with business, research developments with practical insights—to offer industry leaders the information needed to plan and move forward with confidence.

For more information visit:
www.3dasip.org

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