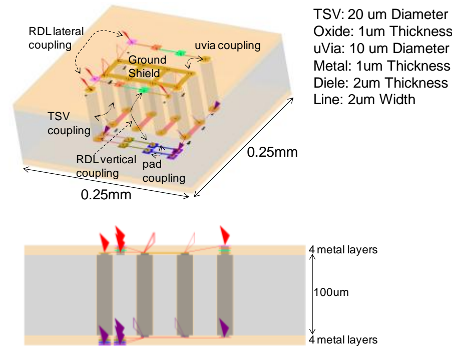
Sphinx 3DPF V3.0 Sparkle sheet

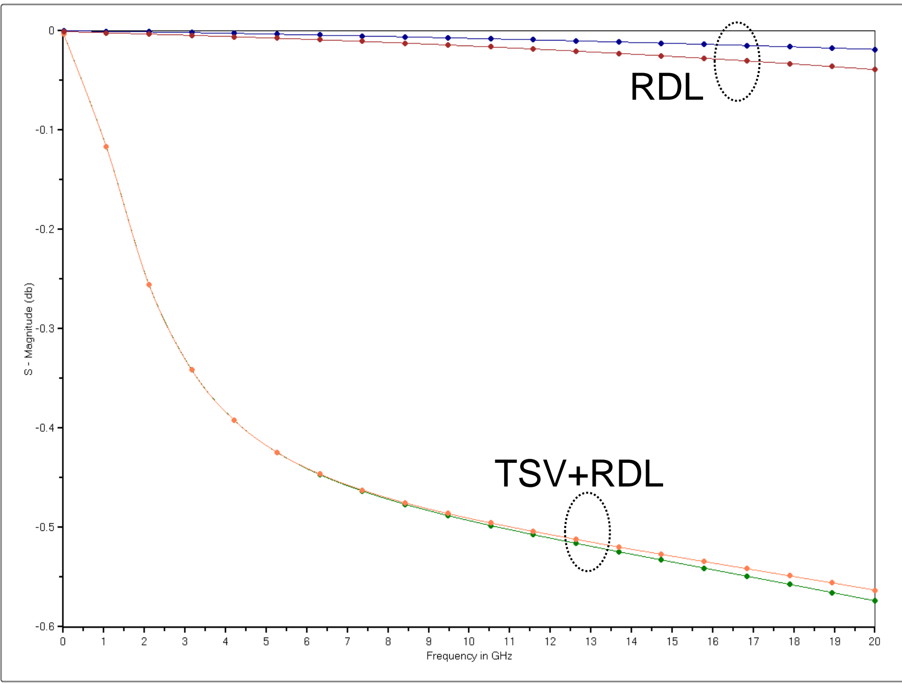
Case 1-3 Responses

E-System Design

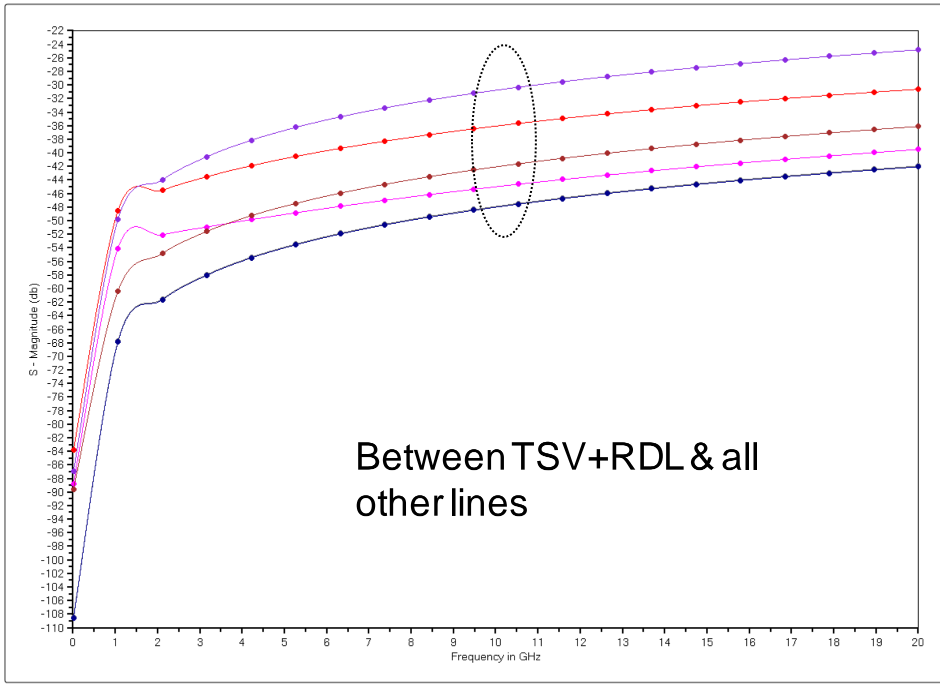
Case 1: TSV with RDL



Insertion Loss



Coupling

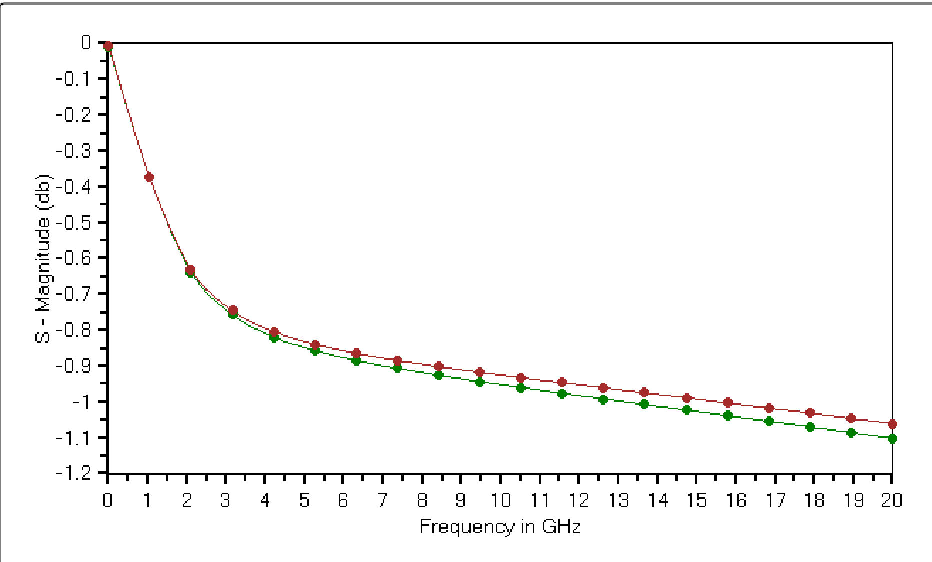


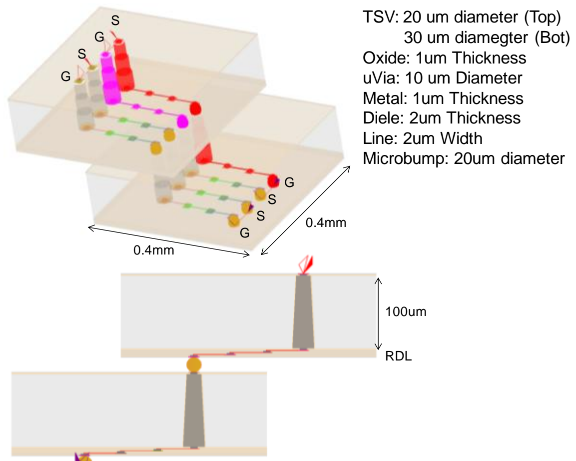
RDL for this structure has minimal IL degradation since they are routed above or below silicon substrate, while TSV/RDL paths have ~14X worse IL

In spite of the ground shield using multiple TSVs, the coupling can still be high. In this example the coupling is between -24 to -48 dB.

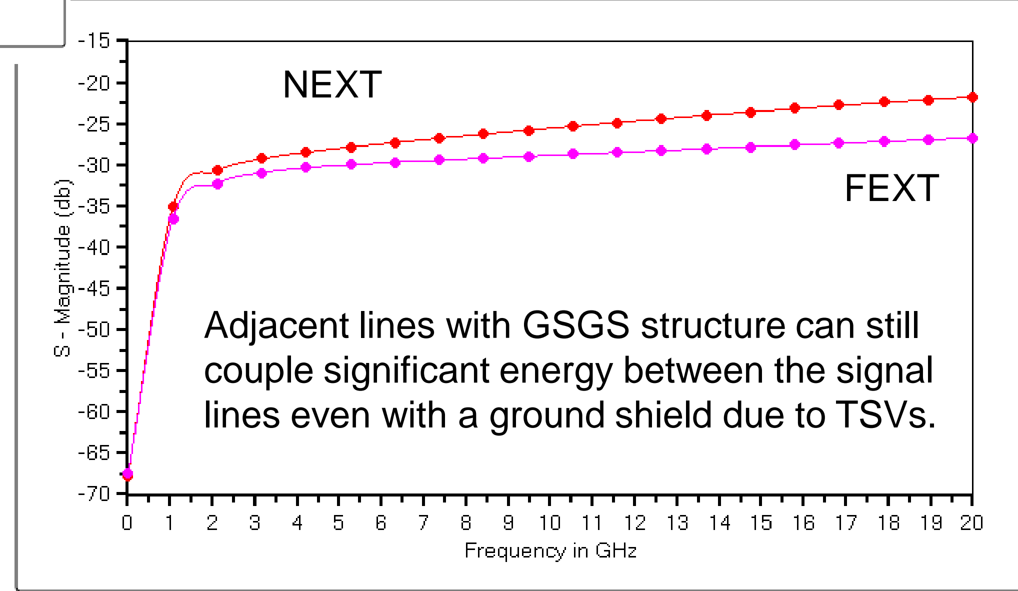
Case 2: Two Chip Stack

Insertion Loss



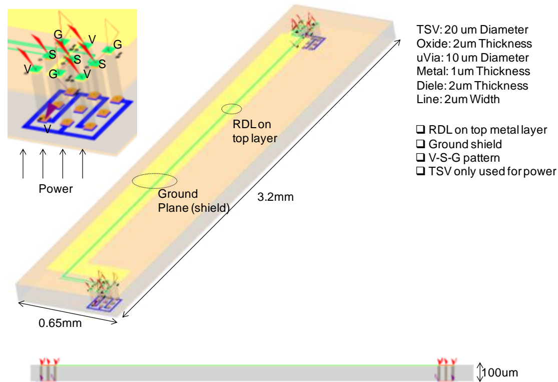


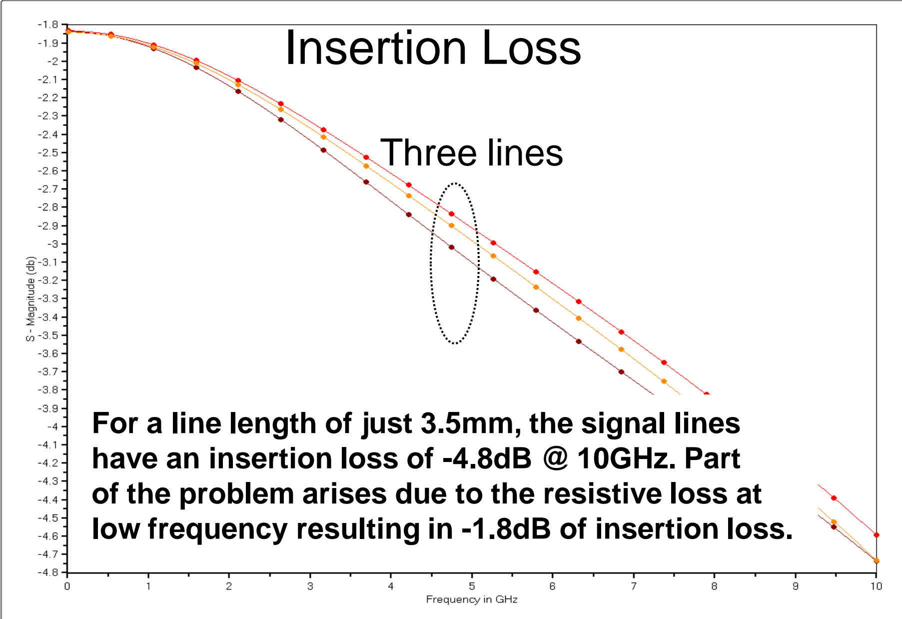
Coupling between Lines

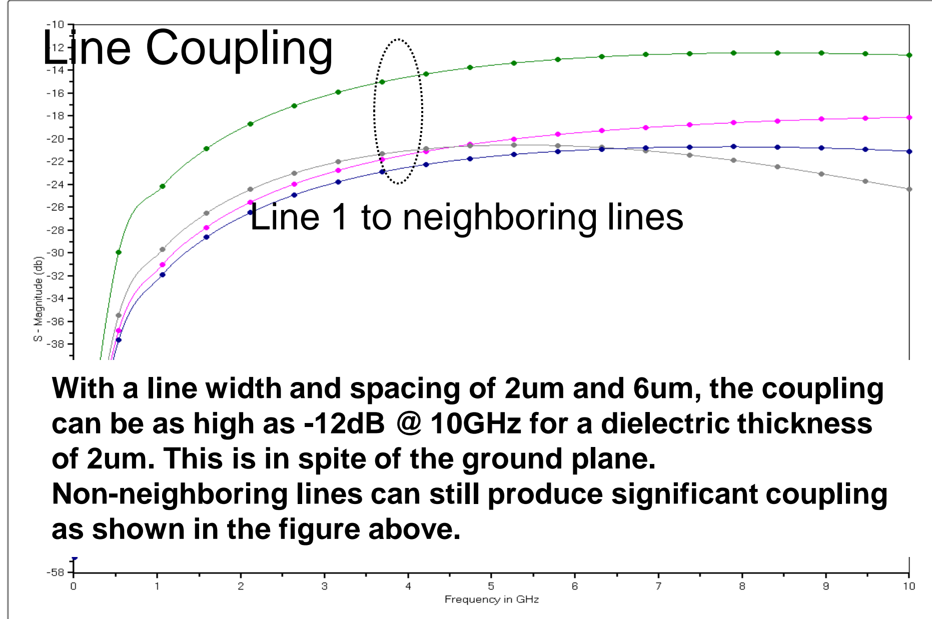


Adjacent lines with GSGS structure can still couple significant energy between the signal lines even with a ground shield due to TSVs.

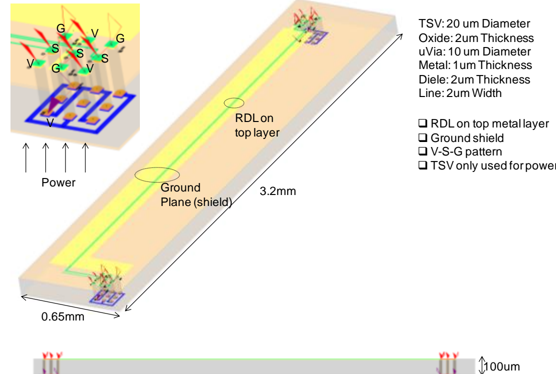
Case 3: Chip-to-Chip with Interposer Signal Analysis

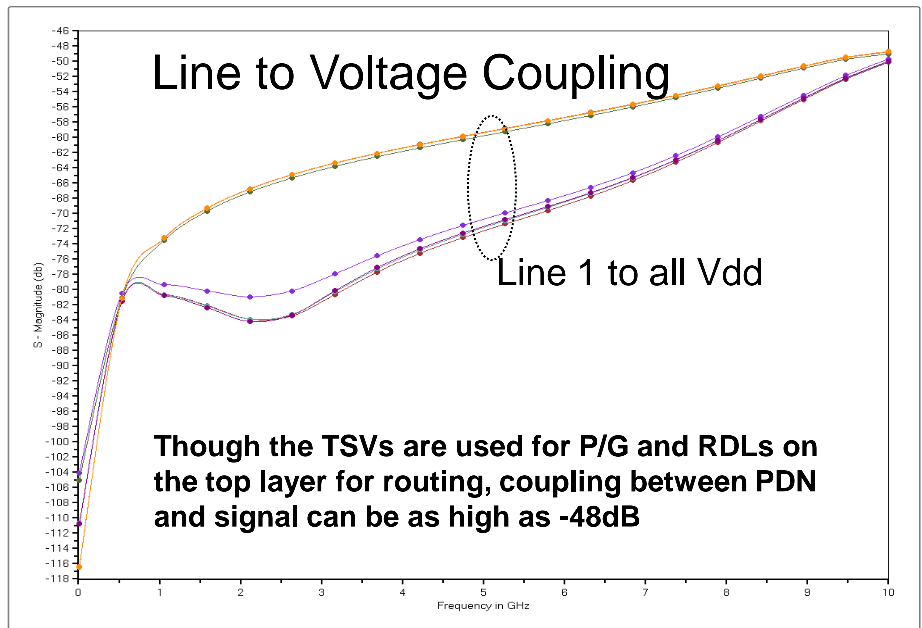


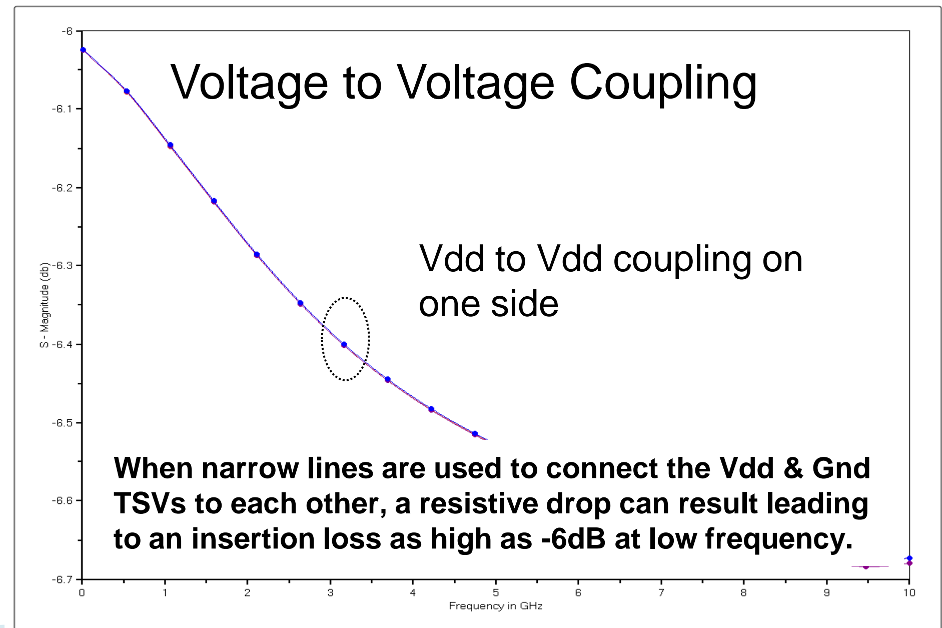




Case 3: Chip-to-Chip with Interposer Power Analysis







Thank you

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