Sphinx 3D PathFinder
"Sphinx 3DPF"

Sphinx 3D Path Finder "3DPF" V4.0

Path Finding is a process of exploring alternatives for determining the optimum mix of structures and technologies prior to implementation. "3DPF" is that tool for 2D, 2.5D and 3D integration.

The goal of Sphinx 3D Path Finder ("3DPF") is to explore all the new technologies available for 2, 2.5 and 3D packaging before costly implementation. 3DPF has been specifically developed for path finding thereby allowing expert and non-expert users to easily construct and accurately analyze complex test structures as they hone their implementation guidelines. The real power of 3DPF is to unleash an organization's staff and imagination to fully explore ALL available options while reducing time, cost, risk and resources required.

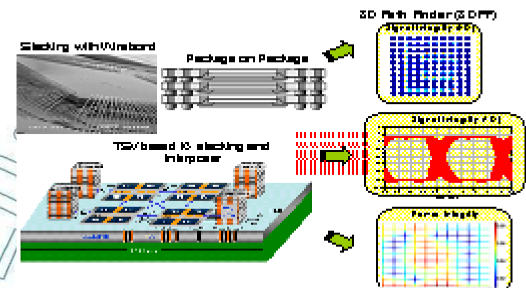

Figure 1: 2.5D and 3D technologies

Supported technologies

3DPF supports various technologies in 2D-2.5D-3D solutions: Through Silicon Vias (TSV), Through Glass Vias (TGV), Redistribution (RDL), Solder bumps (BGA, microbumps), pillars as well as wire bonds. Structures such as: chip stacking, silicon/glass/organic interposers and their interactions can all be constructed and analyzed.

Ultimate freedom to choose

Users can control operating temperature along with many of the physical and material parameters when designing structures that meet the electrical requirements. As test structures are analyzed, users can gauge the effect of implementation changes on the overall performance. When path finding is completed, an optimum solution can be chosen long before costly mistakes are found during backend verification.

Growing staff without hiring

3DPF's intuitive GUI provides a LEGO® block based design approach that enables reusability and fast construction of building blocks that are interconnected with balls, pillars or wire bonds, leading to complex 2D, 2.5D or 3D structures. Non-expert to expert users can quickly adopt the analysis methodology and contribute significantly towards decision making.

What about flows using 3DPF?

The beauty of path finding is that it is at the beginning of the documentation and design flow. Long before logic is designed or transistors are laid out, path finding can help navigate the available technology options. To create flows, 3DPF allows users to create tab delimited ASCII files from scripts, Excel, Word that allow easy support (and documentation) for supporting Design of Experiments (DoE). Both import and export files can be created allowing for easy modification. In addition, 3DPF creates industry standard Touchstone files that can be converted into macro models for Time Domain analysis. Frequency dependent RLGC parameters for via structures are generated along with continuity checks for complex designs

Is Process tuning supported in 3DPF?

For users that define manufacturing process specifications, process parameters can be modified to identify 'sweet' spots for maximizing performance and design yields. Along with a robust design, 3DPF allows for the development of a robust process. The parameterized GUI allows for easy analysis of process corners.

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Does 3DPF have accuracy for the Experts?

Did we forget accuracy? NO. 3DPF's patented algorithm uses method of moments (MoM), specialized basis functions and Partial Element Equivalent Circuit (PEEC) approach thereby accounting for complex parasitic effects due to current flow and charge distribution for both semi-conducting and insulating substrates. 3DPF's accuracy is comparable to full wave electromagnetic (EM) solvers but requires significantly less memory and CPU time as compared to other solvers. Users can EITHER obtain results faster OR can analyze larger structures that otherwise must be 'chopped' to fit into other tools.
Either way: 3DPF can be an asset when introduced into a design flow!

What are Users saying about 3DPF?

"Best technical simulation GUI I've ever used. It is quick, responsive, logically organized, and intuitive....I do really like it" – A large Foundry

"Experiments are much easier to set up than with competing tools, dramatically reducing setup time costs." – A large Semiconductor Company

"Similar to other commercial tool responses but with less CPU time" – A large Semiconductor Company

As EUV, FDSOI, FinFET and 450mm wafer solutions continue to struggle with costs and adoption, the industry is migrating towards 2.5D and 3D packaging based solutions. This is the perfect environment and time for using 3DPF!

As the dimensions of interconnects and thicknesses of the substrates shrink, two major problems arise namely, increased losses and coupling. These issues have to be addressed in the context of Signal Integrity, Power Integrity or combined Signal and Power Integrity modeling. With vertical interconnect structures such as Through Silicon Vias, Through Glass Vias and micro bumps playing a very important role along with redistribution layers, their effect needs to be addressed as well. Power Distribution Networks (PDNs) are critical to minimizing PDN impedances and identifying anti-resonances that can cause increase power dissipation along with increased jitter. Four examples of typical structures that can be analyzed using 3DPF are illustrated on the next page. The results of the analysis are available at: **http://www.e-systemdesign.com/Collateral.html**

Learn more about 3DPF and 3D integration from the book "Design and Modeling for 3D ICs and Interposers". M. Swaminathan and K.J. Han; World Scientific 2013

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Case1 (Figure 2):

A small 0.25mmx0.25mmarea in silicon interposer technology can cause considerable coupling in spite of the ground shield used. The ground shield is in the form of grounded TSVs where the RDL layers are affected by the loss of the silicon substrate.

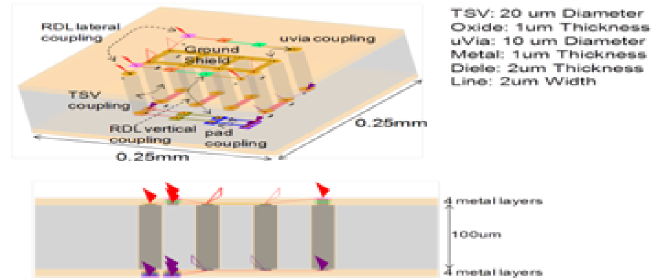

Figure 2: Silicon Interposer in 3DPF GUI

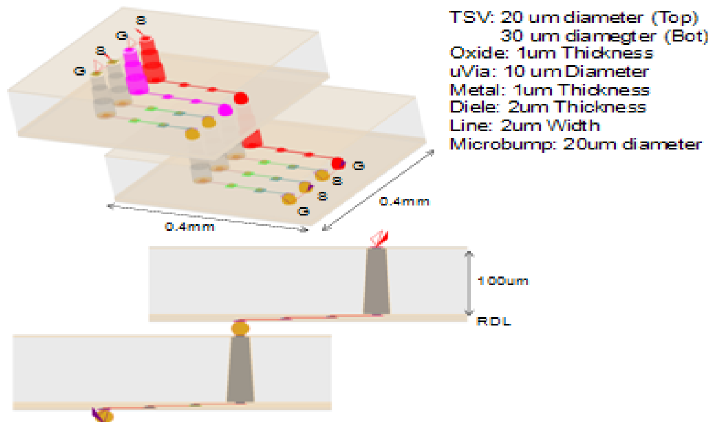

Figure 3: Stacked TSV blocks in 3DPF GUI

Case2 (Figure 3):

TSVs are often tapered due to process conditions with stacking of ICs required t o minimize space and enhance throughput. The ICs are connected through micro bumps along with RDL layers.

Case3 (Figure 4):

RDL can be used to interconnect ICs on the top metal layer with a ground plane to minimize the effect of the silicon substrate. The TSVs can be used only to supply power and ground to the ICs. Narrow width of the RDL induces resistive losses while the presence of the TSVs can amplify the signal to power coupling in spite of shielding using the ground plane.

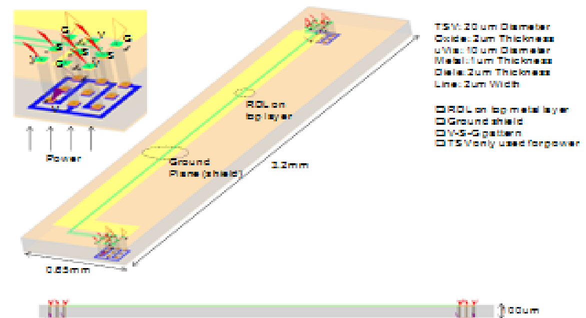

Figure 4: Stacked TSV blocks in 3DPF GUI

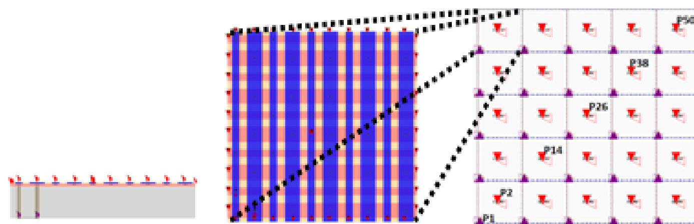

Figure 5a Leaf Cell Profile   Figure 5b Leaf Cell   Figure 5c PDN array (5x5 leaf cells)

Case4(Figure 5):

PDNs are planned early to support a design's requirements and are critical to performance and functionality achieved. 3DPF PDN allows users to quickly explore different alternatives for their IC, Package or PCB PDN. Self and transfer impedances along with PDN noise can be reviewed from simulations.

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Other Path Finding Products in the Family

Why stop at just TSV and CGA block analysis? Sphinx 3DPF foundation allows other capabilities to be easily added with additional licenses for building and analyzing complex Interconnect, Silicon and Glass Interposers as well as Sphinx 3DPF PDN for power distribution analysis. Path Finding represents analysis at an early exploratory stage where decisions need to be made on the choice of packaging technology, assembly technology, interconnection technology and many more. The Sphinx 3DPF product family focuses on electrical response as the performance metric for path finding. Below are additional licenses and descriptions that can be purchased to expand Sphinx 3DPF baseline capabilities. The present and future Sphinx product offerings are shown in Figure 5.

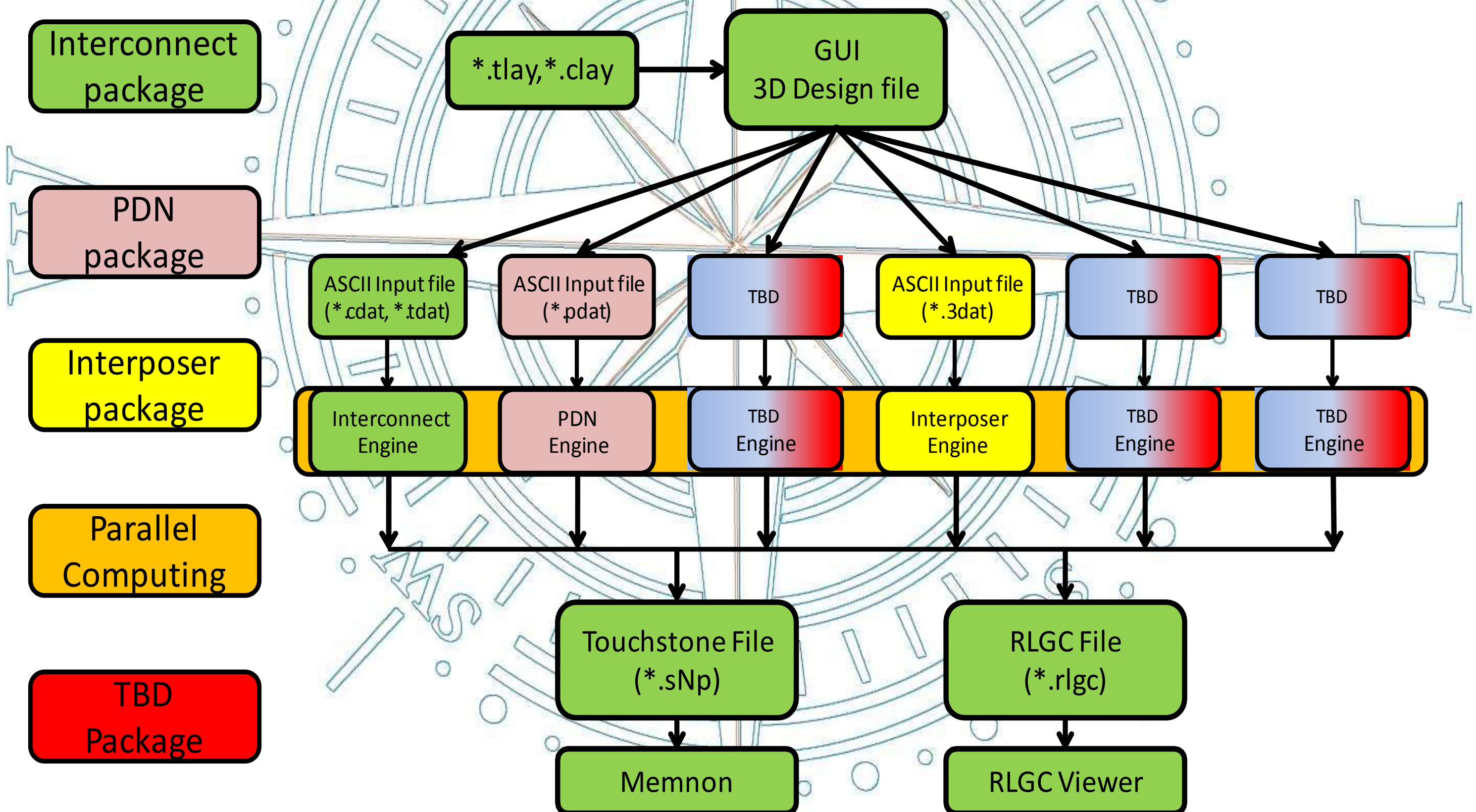

Figure 5 Sphinx 3DPF Product Family (V4.0)

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Interconnect**, **Interposer**, **PDN and ***Parallel Computing*** products are available today and focus on Signal/Power Integrity.

Sphinx 3DPF Interconnect package enables the analysis of interconnect structures in the presence of dielectric and semiconducting materials. Included in the electromagnetic analysis are redistribution layers (RDL), dielectric vias, through silicon vias (TSV), via tapers, non-uniform metal and many more where signal responses, signal-to-ground ratios, crosstalk, return path discontinuities (RPDs), temperature and other effects can be evaluated.

Sphinx 3DPF Interposer package enables the connection of chips to interposer through wirebonds, solder bumps or micro bumps and package to package connections through solder balls or pillars. So the *Interposer* product can be used to analyze a standalone glass or silicon substrate for chip to chip performance or stack packages to evaluate its overall response where the performance metric can either be insertion loss, return loss or cross talk.

Sphinx 3DPF PDN software package uses a unique algorithm for PDN analysis across chip, package or pcb that provides very high accuracy. Results are in the form of impedance or scattering parameters. This product can be very useful for:

i) comparing impedance parameters with the target impedance
ii) assessing the impact of resonances in the PDN
iii) re-evaluating the design for making suitable modifications for reducing the PDN impedance.

The premise behind creating a power distribution network (PDN) is to check for the impedances and resonances to determine the frequencies where they exceed a target value. The PDN response is then converted to a spice netlist for time domain analysis to evaluate power supply noise and its impact on transistor performance. Since the chip, package and pcb can all alter the PDN response over specific frequency ranges, their individual and combined effects need to assessed.

Sphinx 3DPF PDN outputs a touchstone file that can be converted into a condensed spice netlist, which provides a behavioral representation of the power distribution network of the system.

Sphinx 3DPF Parallel Computing package allows user to use as many CPU's that are contained within their machine offering significant decreases in time to analyze based upon number of CPUs used. As an example, we have run various tests and have seen 3.7X improvement using 4 CPUs.

For more information on 3DPF visit us at www.e-systemdesign.com

Protected under US Patent #8,352,232 with other patents pending.

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