E-System Design inc.

www.e-systemdesign.com

Why Frequency Domain Analysis?

Most engineers were trained using SPICE, a very old friend that continues to be the dominant simulation tool for many applications. Although frequency analysis has been used for many years, most of us remember how time consuming it was to create Smith Charts showing a circuit's response in impedance (Z), admittance (Y) or scattering (S) parameters. Over time, improvements in methodology and tools have made frequency analysis much easier to perform. Let's evaluate the time to results (TTR) between the two different methods and compare the results.

Time domain analysis uses a typical V (or I) vs. time. Today's measure of time is typically in picoseconds or nanoseconds, not frequency. The user must create a 'netlist' that incorporates all components within their design for accurate simulation. To create this 'netlist' requires extracting portions of their available design, retrieving latest IBIS or SPICE models from various vendors and then combining these into a workable netlist that simulates with the same SPICE version they intend to use. A non-trivial task given the size of current designs and the increasing percentage of IP purchased from 3rd party suppliers. Once a netlist has been created, the user then must create 'test patterns' used to stimulate the design and capture the responses at identified nodes. At last, the user can start to analyze how their entire design and the components (ICs, printed circuit boards, packages, resistors, capacitors, inductors, power supplies, etc) all work together.

But what if we were able to test components without all of the work required for time domain analysis?

Frequency domain analysis helps accelerate and parallelize development activities. Rather than waiting for the entire design (IC/SoC, pc board, etc) to be completed, designers can start to validate parts of their design long before other components are finalized. Finding and resolving issues long before they become critical in their schedule and reducing the risk to market introduction.

Sphinx, a signal and power integrity co-simulator, allows designers to effortlessly analyze their designs. A simple process of reading in their design, adding ports to various signals or planes in their design and then stating what frequency range to use in analysis is all that is required. The user does not need to: find all the SPICE/IBIS models; hand-edit the netlist or create stimulus patterns. Once the analysis is finished, the user can view Z, Y or S parameters in a simple to understand linear parameter vs. frequency graph.

Depending upon the ports added, users can validate voltage island isolations, substrate noise, cross talk between signals, insertion and return loss on signals, differential signal integrity, frequencies that cause anti-resonances thereby preventing the design from working correctly. In addition, voltage distribution and DC analysis can be easily simulated and reviewed for issues and problem areas.

Just by a simple 3 step process. Results can be seen within a day and this includes ALL preparation work. Does this mean that time domain analysis can be avoided and thrown away? The simple answer is no. But by inserting frequency analysis into your design flow, many issues can be identified and resolved long before time domain analysis is required. This allows the designer to perform parallel analysis on de-populated pc boards and packages long before the entire design has been completed. Once these other items have been finalized, frequency analysis can also be used.