What's Missing in 3D Packaging Today?

A Workshop to Accelerate 3D Package Path Finding

Date: April 11, 2012

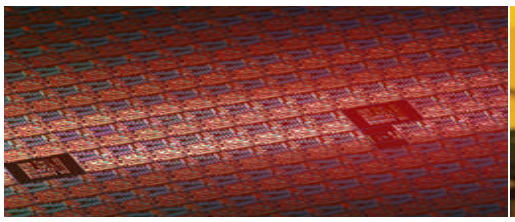
Location: Altera Headquarters, 101 Innovation Drive, San Jose, CA

The SEMATECH 3D Enablement Center is hosting a one-day workshop on April 11th, 2012 at Altera Headquarters to discuss how to accelerate path-finding in the interactions between package, interposer, stacked dies, and system issues.

Speakers from Georgia Tech., Cadence Design Systems, Mentor Graphics, and companies from the OSAT community will present their views in the morning and a round table discussion will be held in the afternoon along with representatives from Qualcomm, Microsoft, LSI Logic, IBM, Altera, Global Foundries, Analog Devices, to crisply identify what's holding back high volume of 3D design starts from a packaging stand point.

WHO SHOULD ATTEND? Semiconductor Industry Association member companies or SEMATECH member companies, EDA companies, OSAT companies, and architects or designers who are involved in tradeoffs in Package Design, Selection and Integration in the context of 3D design.

The workshop is by invitation only, and we hope that you will able to join us. Please contact kumar@siliconideas.net or sitaram.arkalgud@sematech.orgwith your name and company affiliation if you would like to attend. We will need to receive your RSVP by April 1st 2012.



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The 3D Enablement Center

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