Designing Interposers - Electrical Challenges and Potential Solutions

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Abstract

Over the last several years, the buzzword in the electronics industry has been "More than Moore", referring to the embedding of components into the package substrate and stacking of ICs and packages using wirebond and package on package (POP) technologies. This has led to the development of technologies that can lead to the ultra-miniaturization of electronic systems with coining of terms such as SIP (System in Package) and SOP (System on Package). More recently, the semiconductor industry has started focusing more on 3D integration using Through Silicon Vias (TSV). This is being quoted as a revolution in the electronics industry by several leading technologists. 3D technology, an alternative solution to the scaling problems being faced by the semiconductor industry provides a 3rd dimension for connecting transistors, ICs and packages together with short interconnections, with the possibility for miniaturization, as never before. The semiconductor industry is investing heavily on TSVs as it provides opportunities for improved performance, bandwidth, lower power, reduced delay, lower cost and overall system miniaturization. Interposers play a very important role in such 3D integrated systems since they act as the conduit for supplying power, interfacing to the external world and handling the thermal management for 3D IC stacks.

Two different technologies are being proposed for the interposer today namely, silicon and glass. Though glass provides a low loss substrate solution it has its disadvantages which can be corrected using silicon. Similarly, silicon has several performance advantages but is limited due to the semiconductor properties of the substrate which can be corrected using glass. So, which provides a better alternative from an electrical performance standpoint – silicon or glass?

This presentation tries to address this question by looking at the electrical challenges associated with the design of interposers. Since, this is work in progress, some potential solutions are proposed.

Reference:

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